

# Comet Lake S UDIMM(3200) CMP-H Reference Validation Platform

**Customer Reference Board Schematics**

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***Revision 0.7***

***October 2019***

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## ***Revision History***

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<b>Document Number</b>	<b>Revision Number</b>	<b>Description</b>	<b>Revision Date</b>
615704	0.7	Initial Schematics	October 2019

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55	DISPLAY - DP CONNECTOR 1, CMC & ESD																																																																																																																																																																																																																																																											
56	DISPLAY - DP CONNECTOR 1, HDMI INTEROP																																																																																																																																																																																																																																																											
57	DISPLAY - DDI2 PORT, AC CAPS																																																																																																																																																																																																																																																											
58	DISPLAY - HDMI CONN 1, RETIMING LEVEL SHIFTER																																																																																																																																																																																																																																																											
59	DISPLAY - HDMI CONN 1, CMC & ESD																																																																																																																																																																																																																																																											
60	DISPLAY - DP_HDMI_COMBO																																																																																																																																																																																																																																																											
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63	DISPLAY - LSPCON O/P SERIES RESISTOR																																																																																																																																																																																																																																																											
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66	DISPLAY - EDP, AC CAP & CMC																																																																																																																																																																																																																																																											
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196	BLANK
197	BLANK
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199	BLANK
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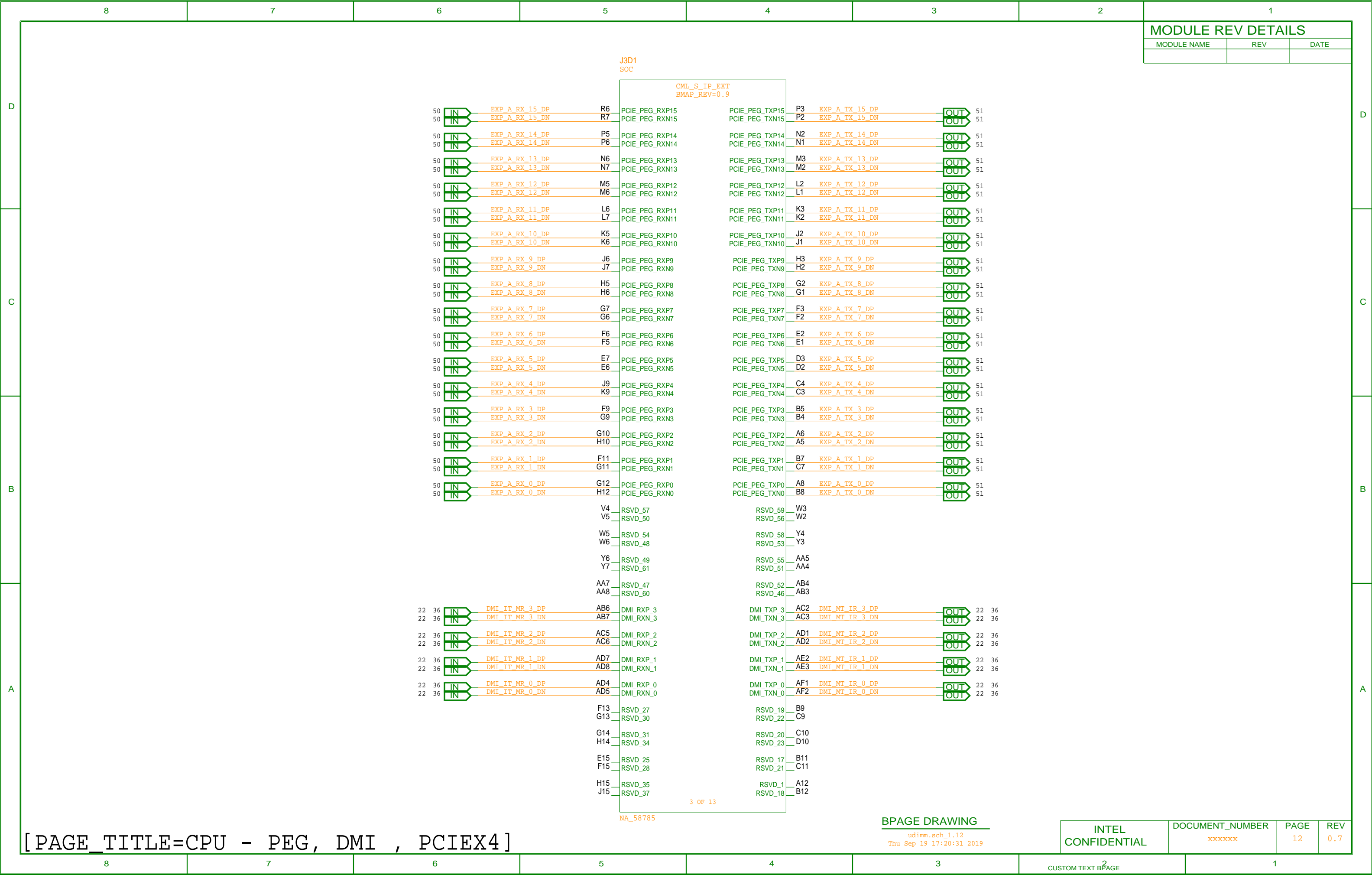
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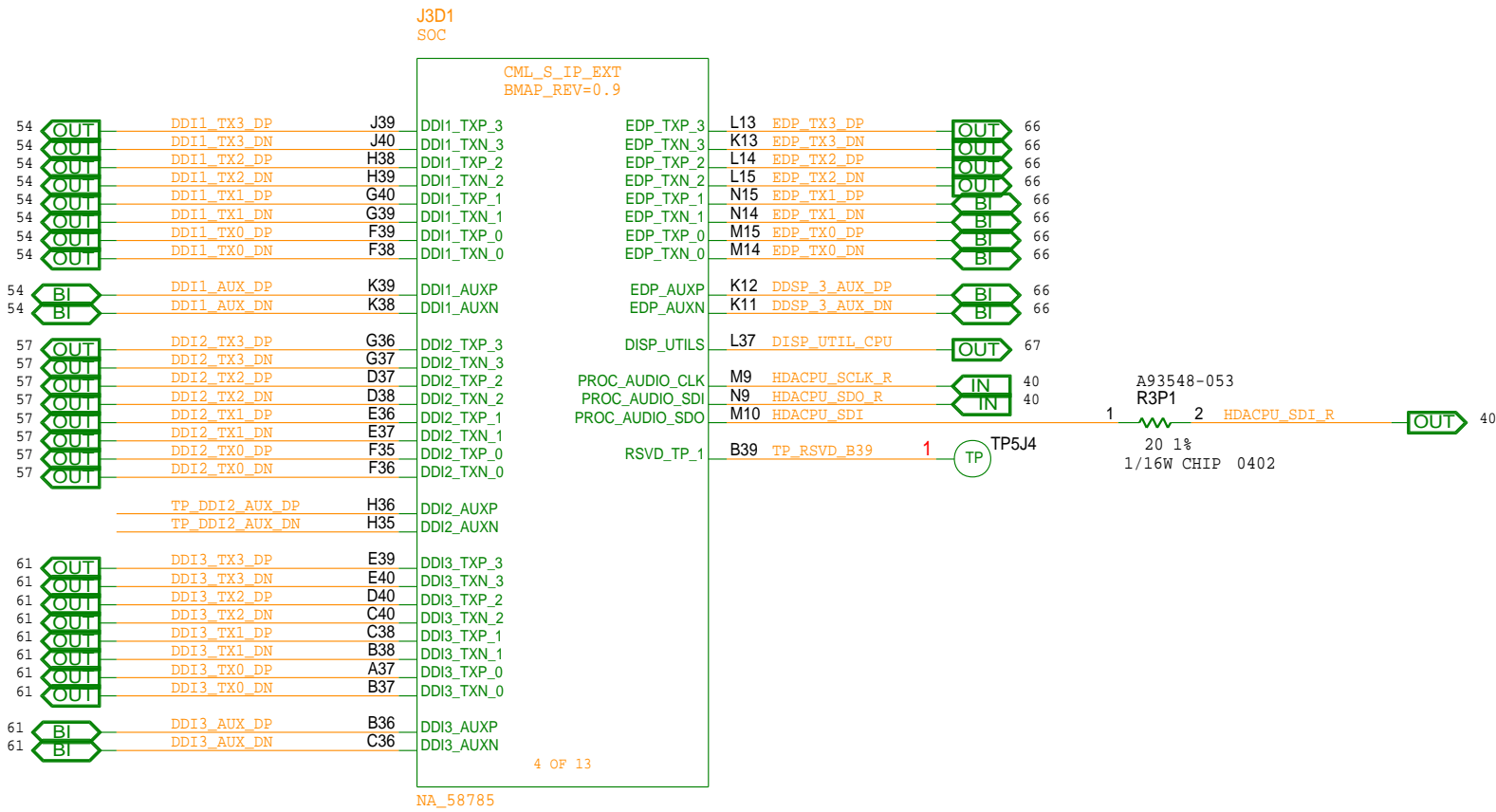
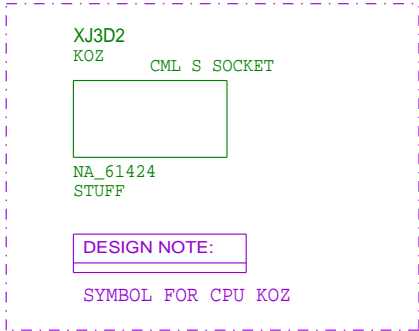


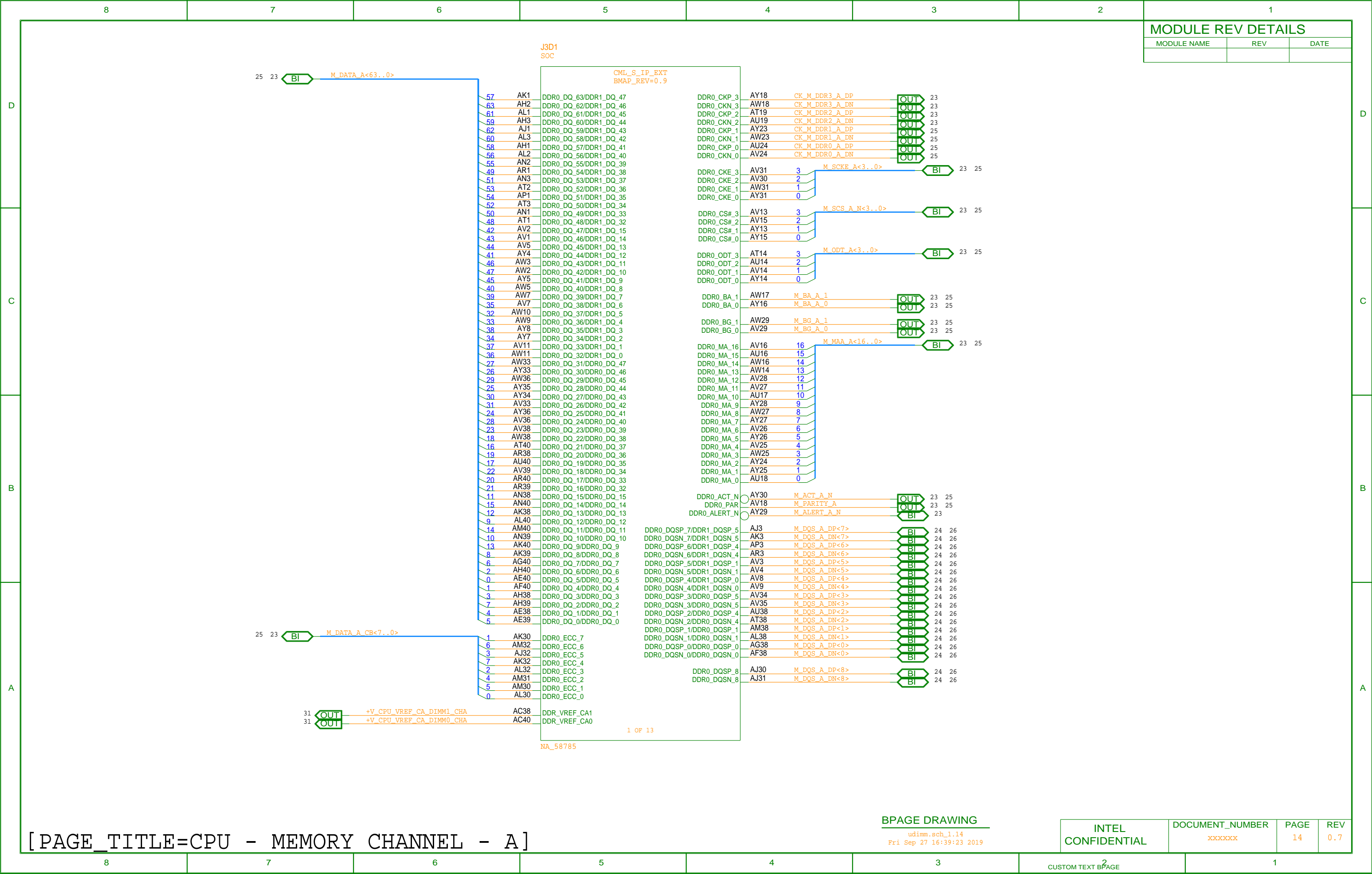
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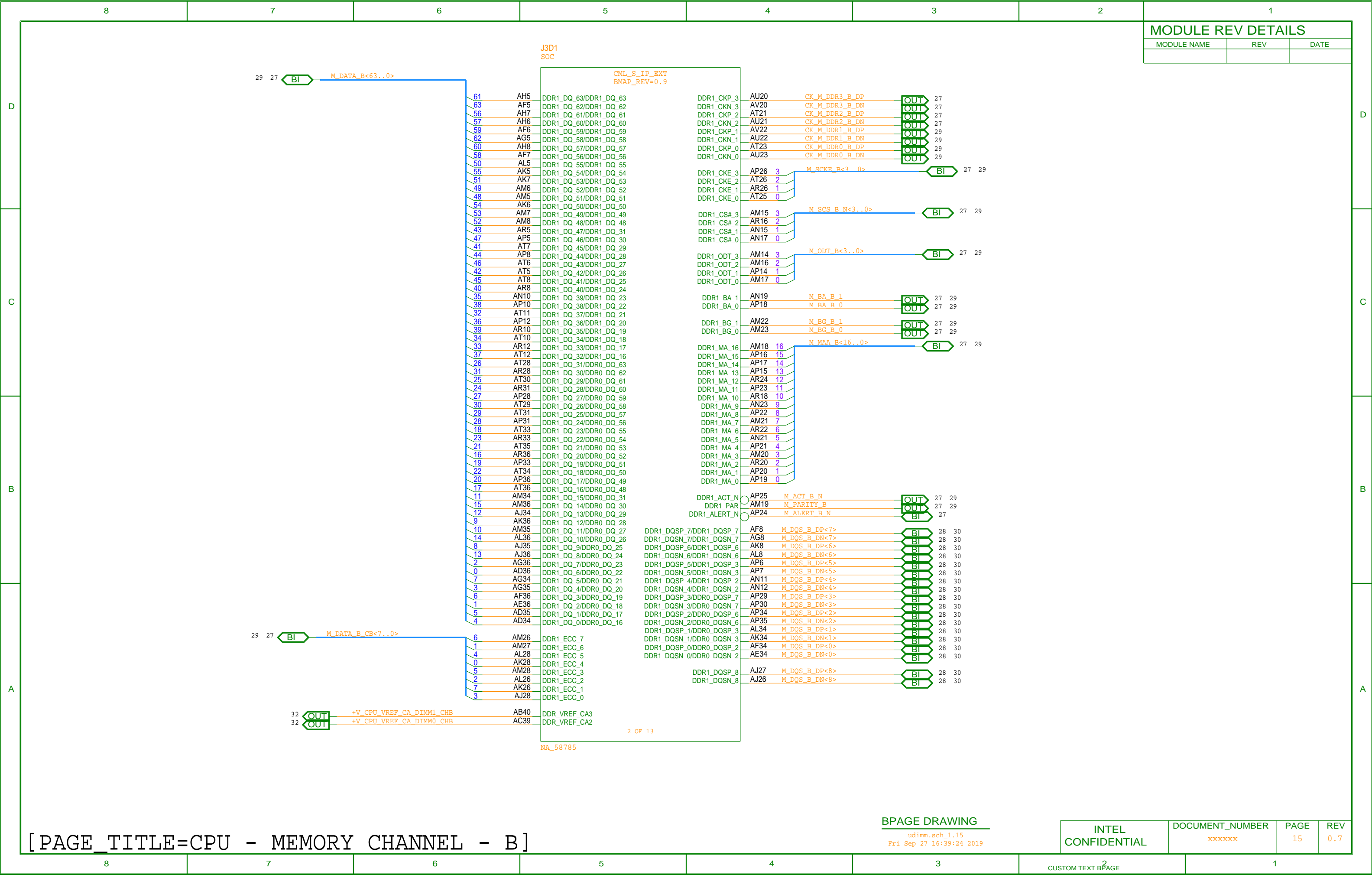
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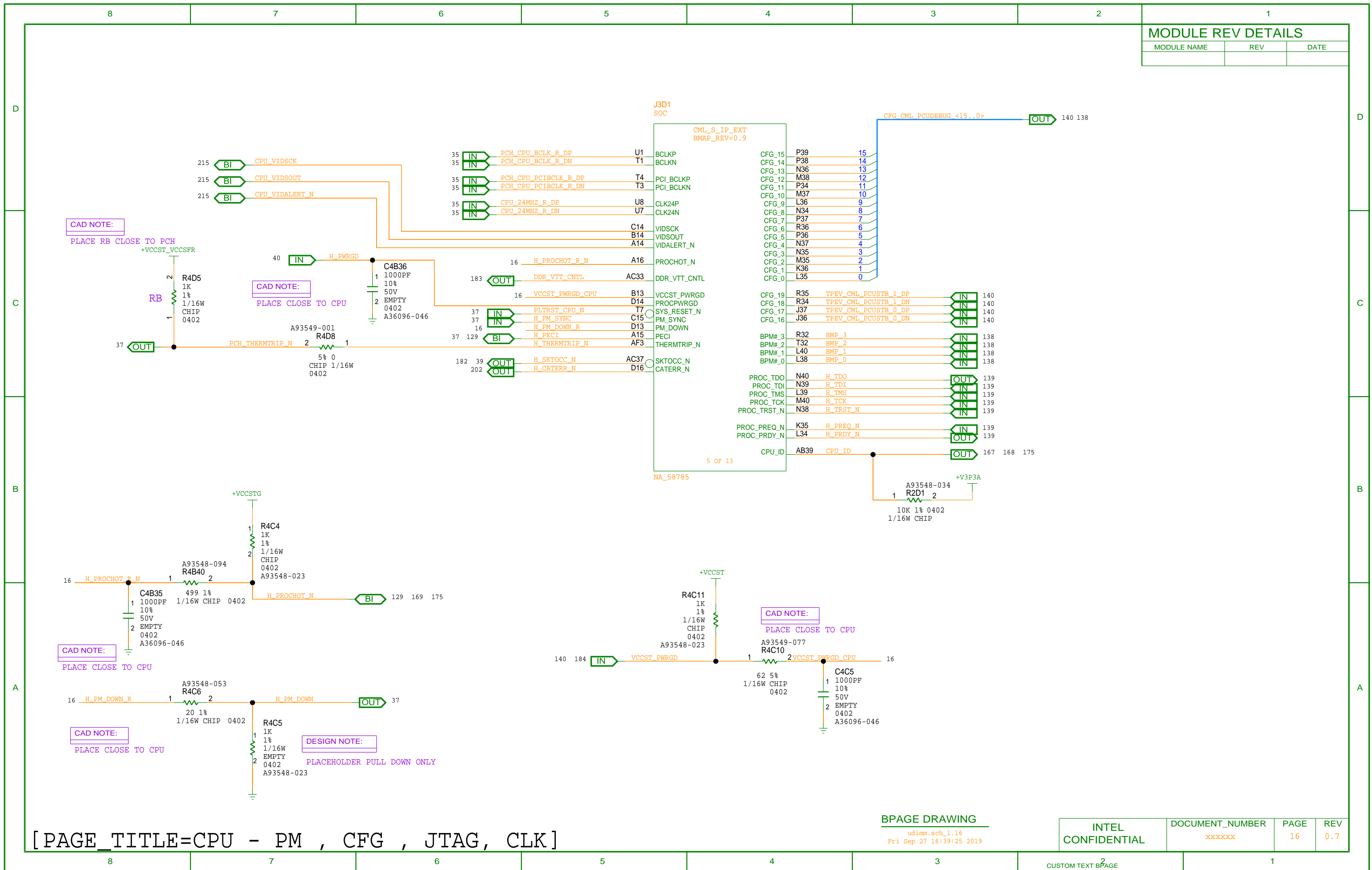
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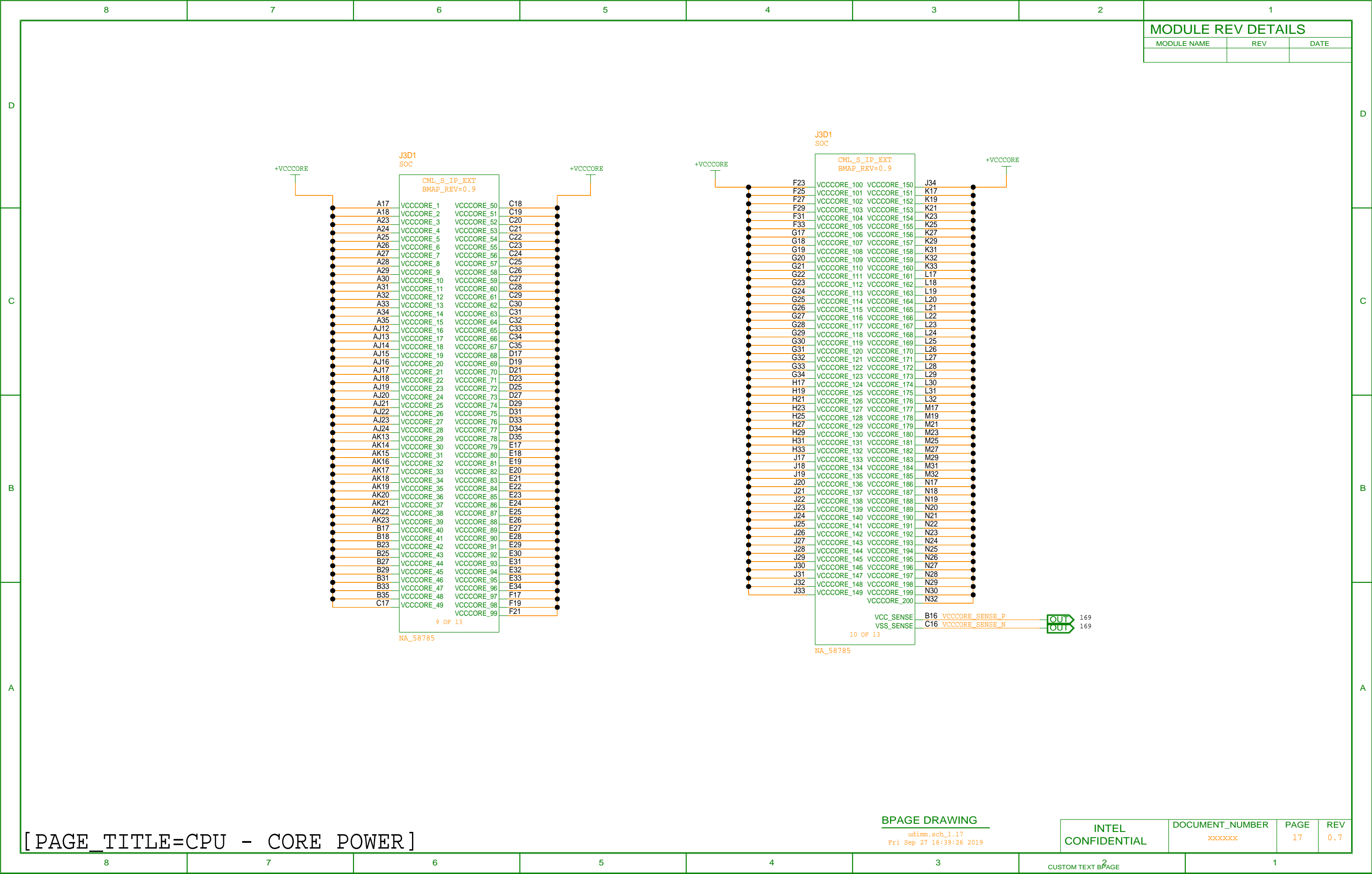
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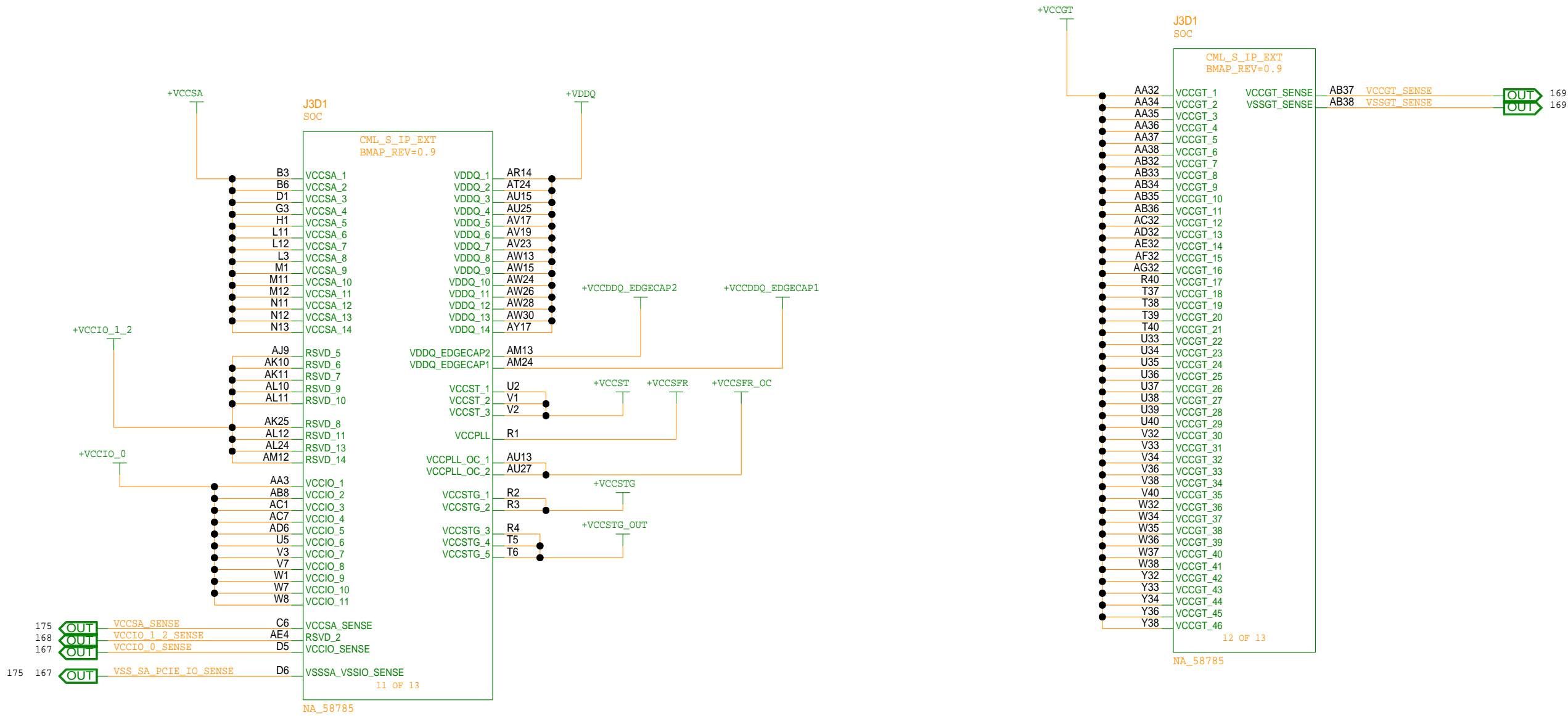
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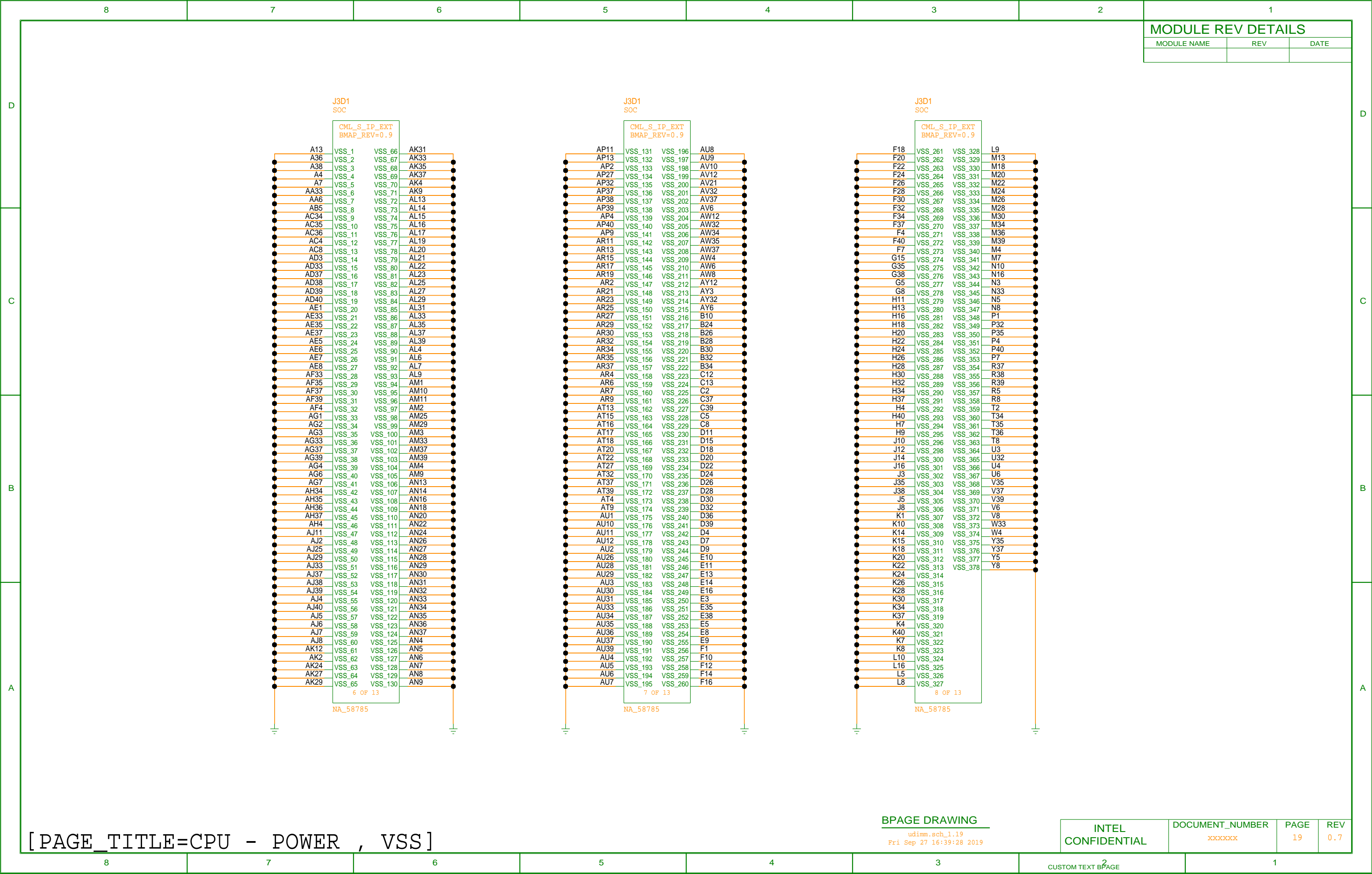
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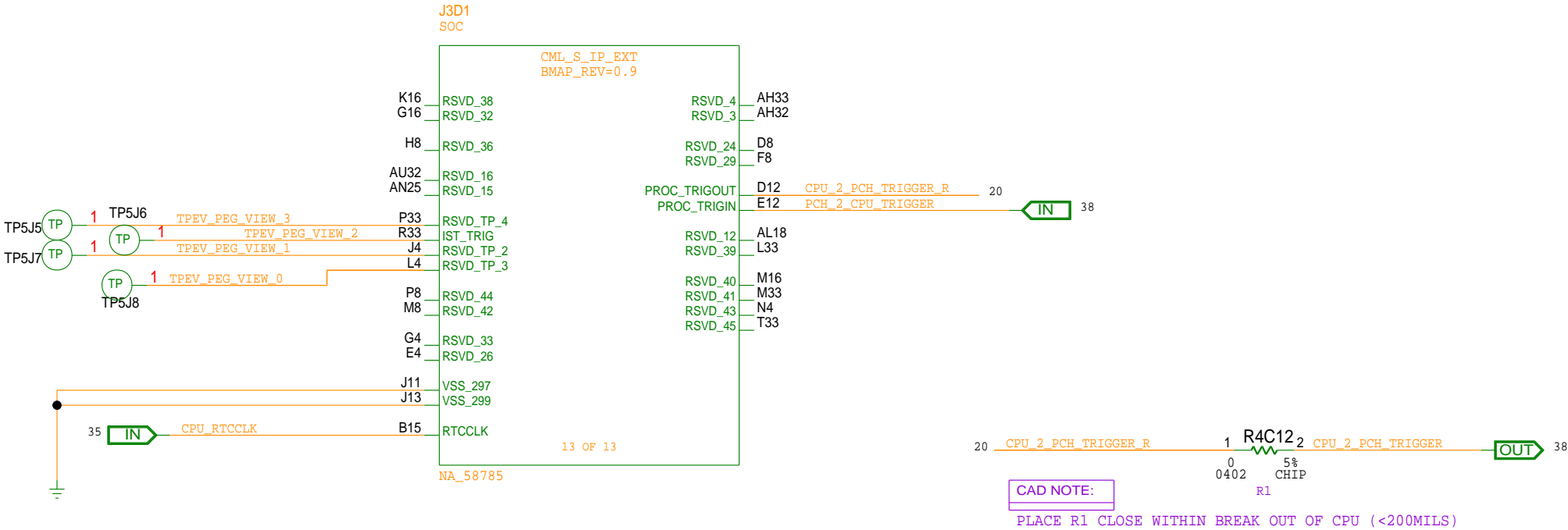
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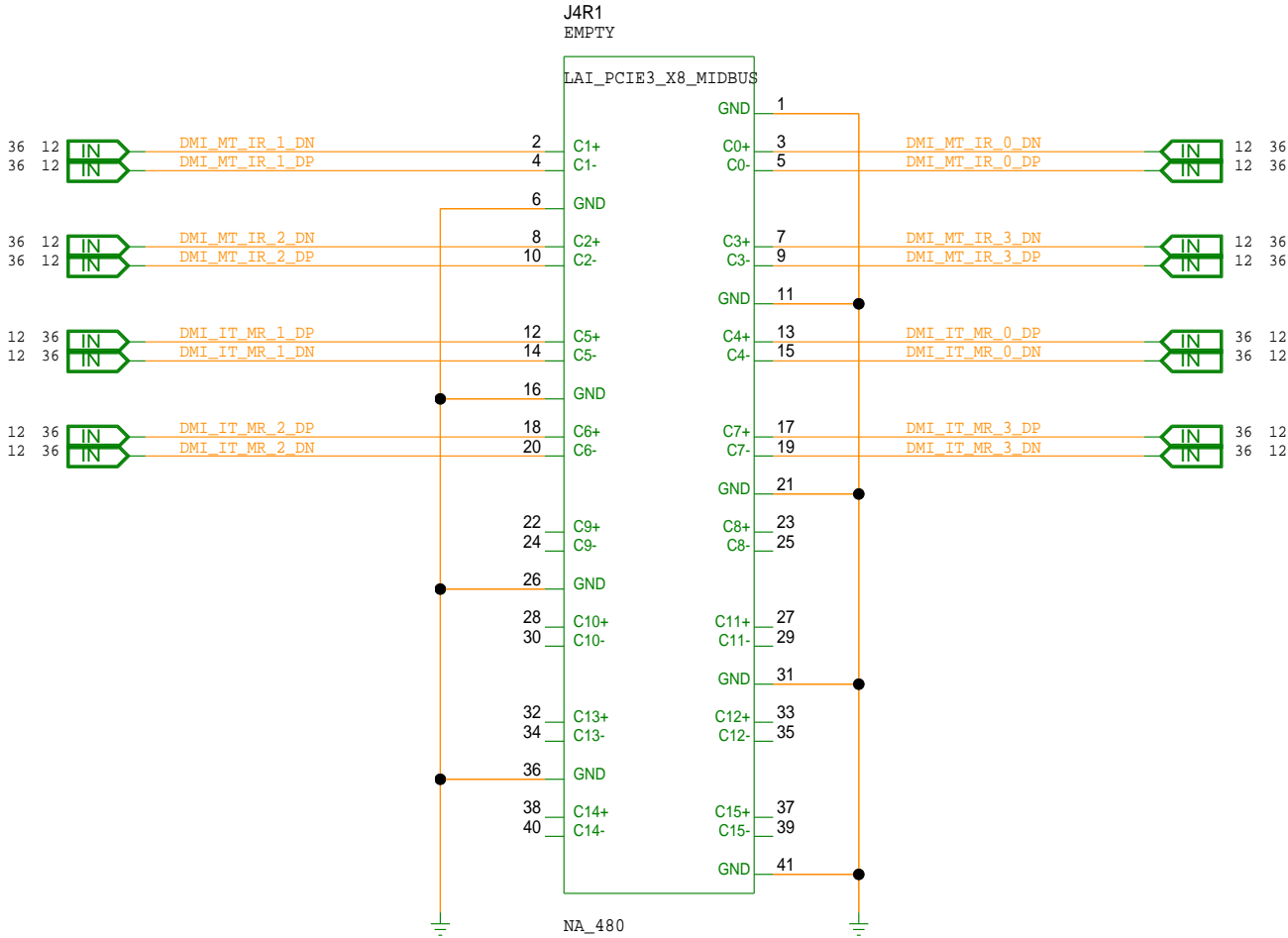
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'EVENT\_N': INDICATES THERMAL EVENT ON DIMM.



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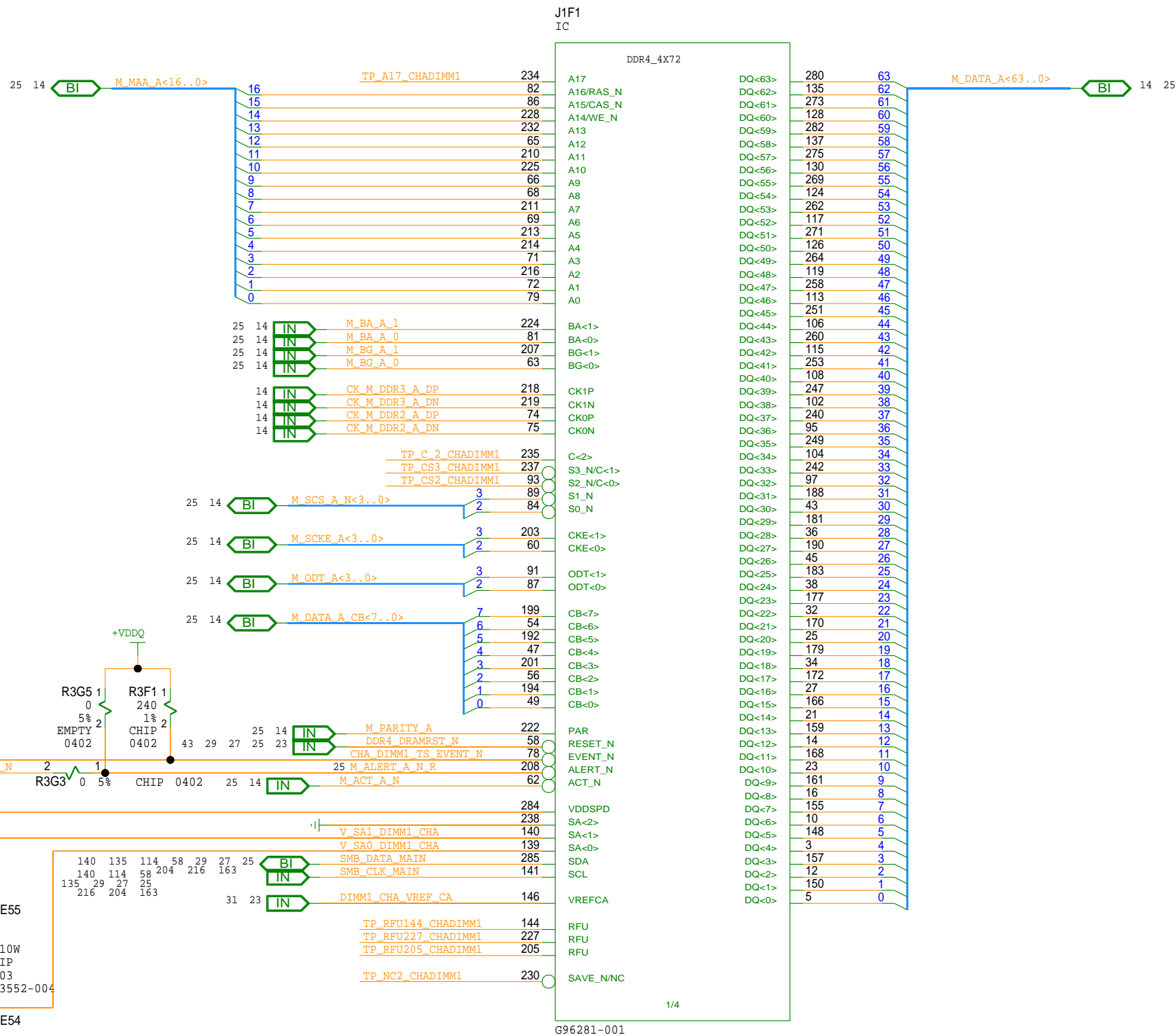
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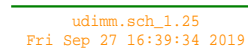
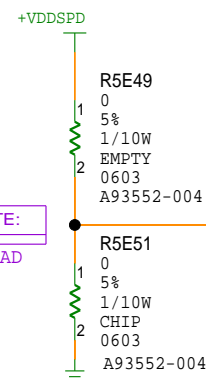
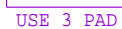
CH A VDDQ\_VTT DECOUPLING CAPS



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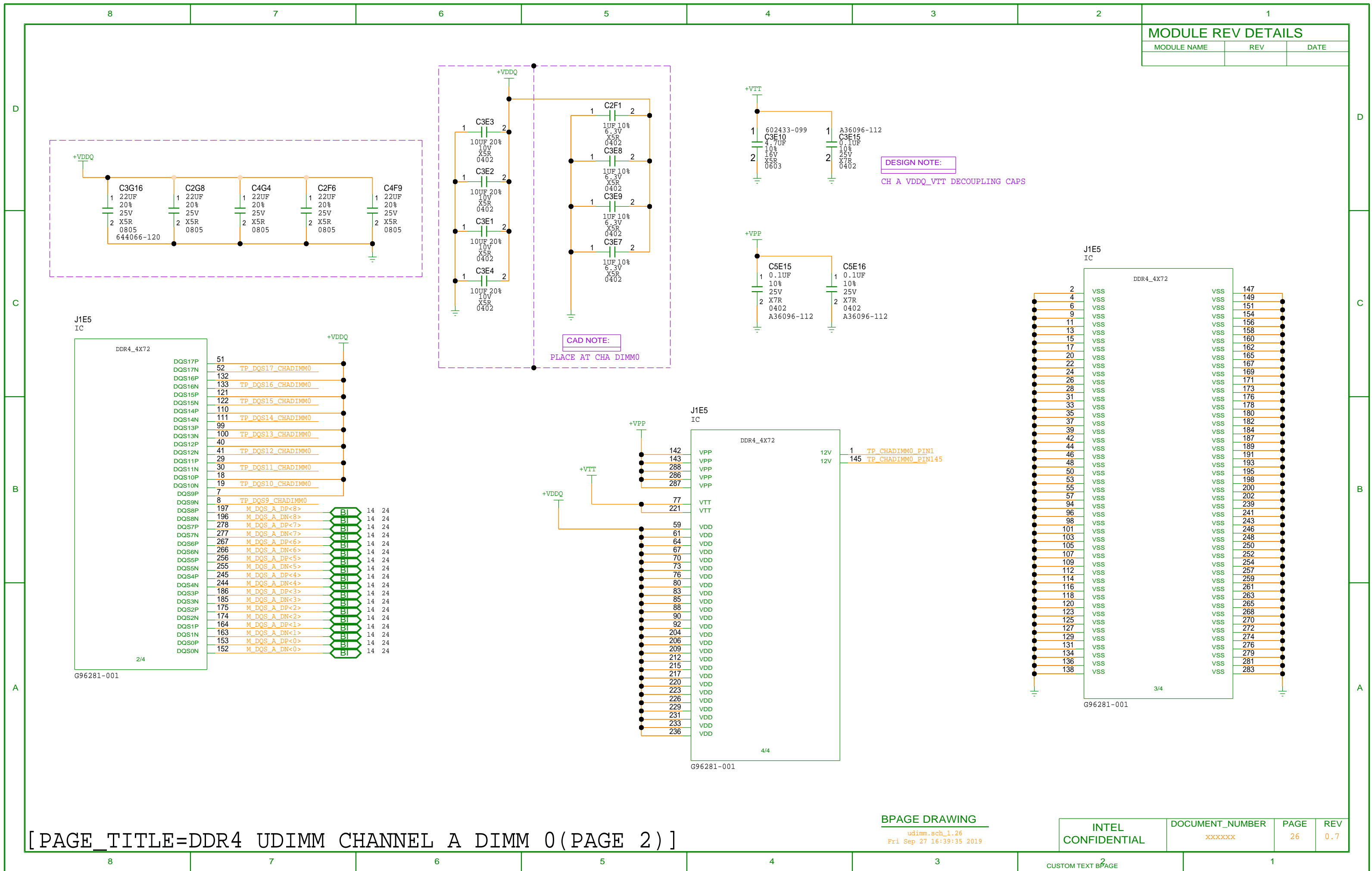
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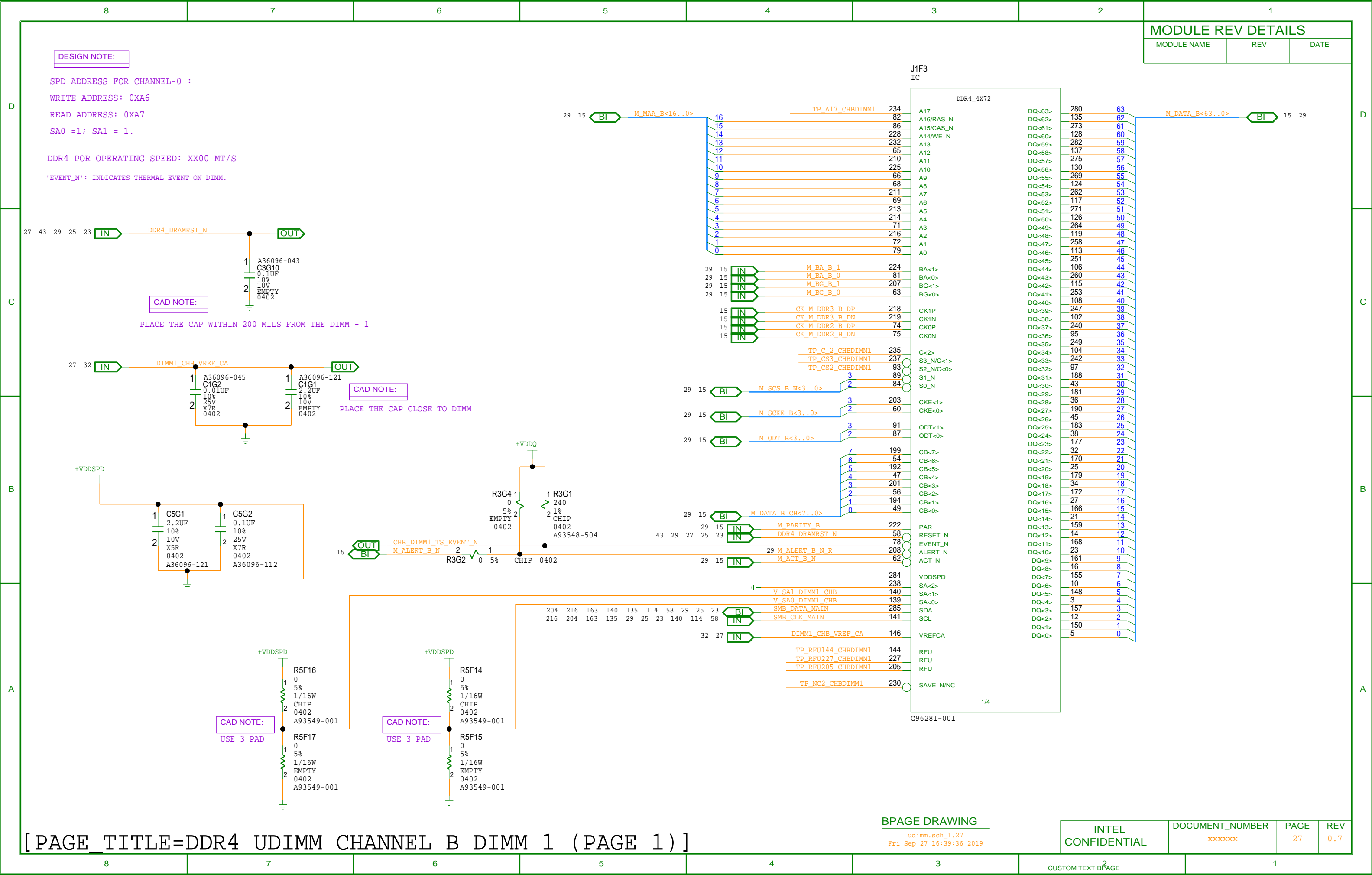
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This diagram illustrates the electrical schematic for Channel B DIMM 1, specifically focusing on the DDR4\_4X72 IC and its associated power and signal connections.

The main components shown are:

- J1F3 IC**: The primary interface component connecting the DIMM to the system bus.
- DDR4\_4X72 IC**: The memory module being populated.
- CAD NOTE**: PLACE AT CHB DIMM1
- DESIGN NOTE**: CH B VDDQ\_VTT DECOUPLING CAPS

The schematic details the following connections and components:

- VDDQ and VTT Decoupling**: Multiple capacitors (C3G1-C3G8) are connected to +VDDQ and +VTT rails to provide stable power during transitions.
- VPP Decoupling**: Capacitors C5G3 and C5G4 are connected to +VPP to decouple the programming voltage.
- DQS Signal Connections**: DQS signals (DQS1P-DQS17P) are routed through J1F3 to the DIMM pins.
- M\_DQS\_B DP<N>**: Memory Data Strobe (MDS) signals for Bank 0 (DP<0>) through Bank 7 (DP<8>) are connected to the DIMM pins.
- VDD and VSS Connections**: Power and ground connections for the DIMM are established via J1F3.

The diagram includes detailed pinouts for J1F3 and the DDR4\_4X72 IC, showing the mapping between the board traces and the component pins.

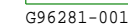
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EVENT\_N': INDICATES THERMAL EVENT ON DIMM.



CAD NOTE:

USE 3 PAD

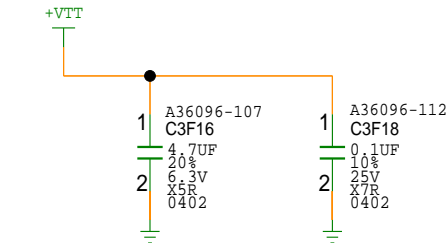
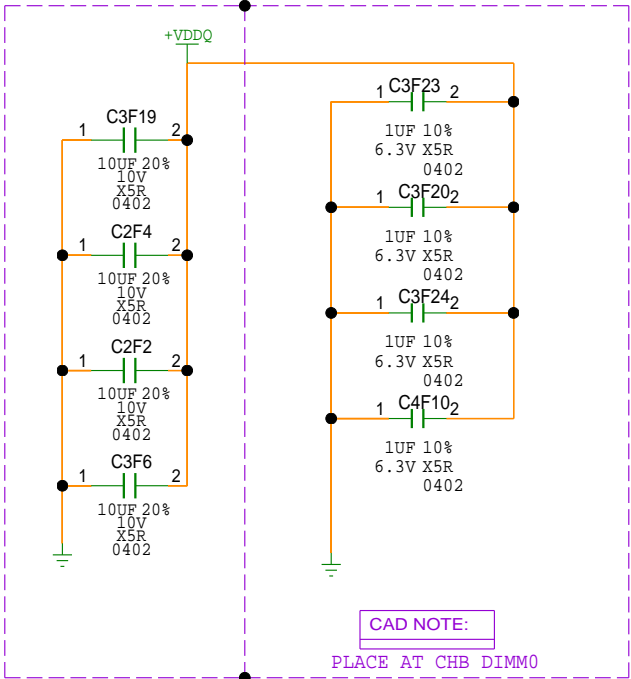
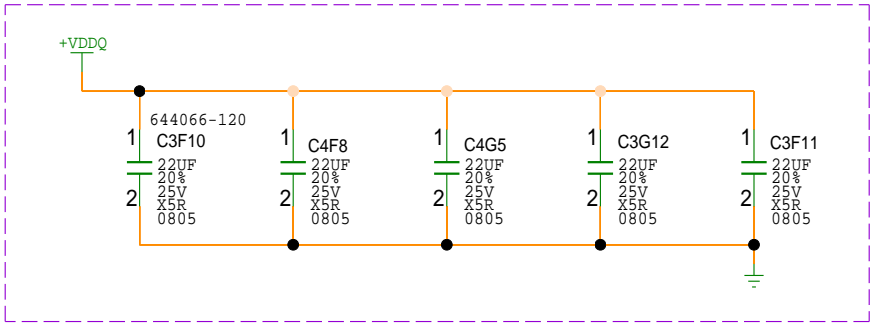


## REV

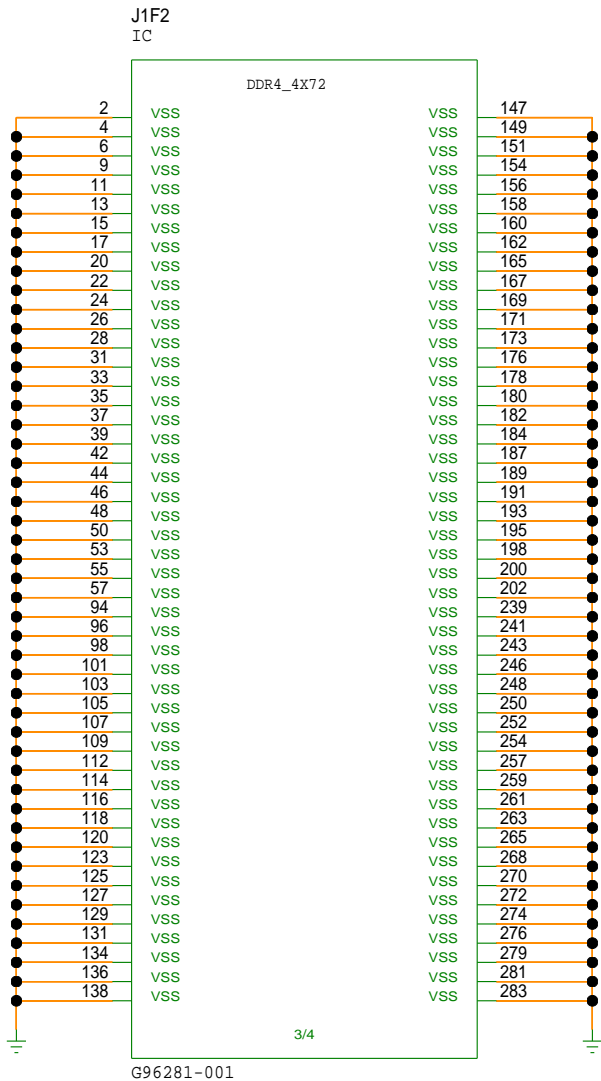
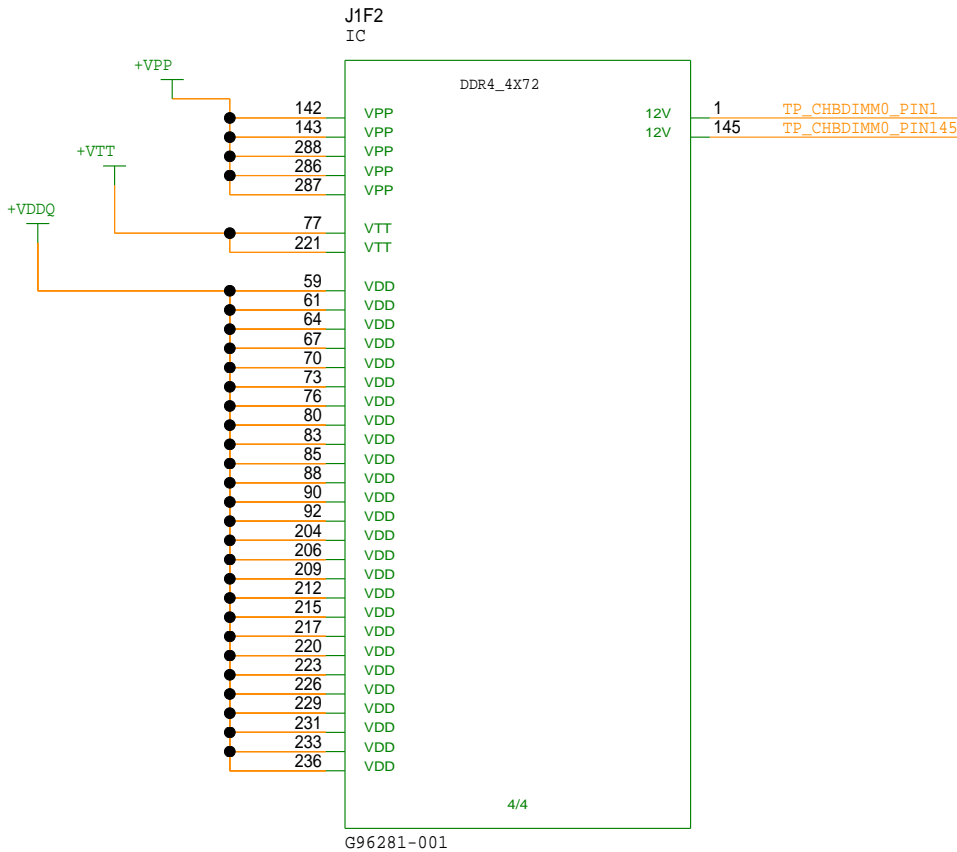
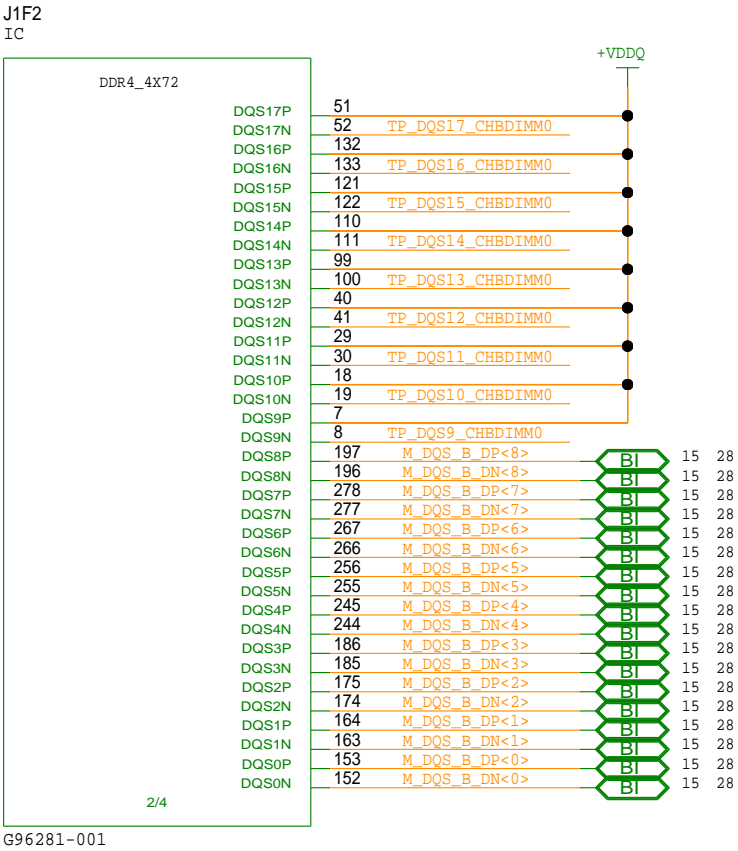
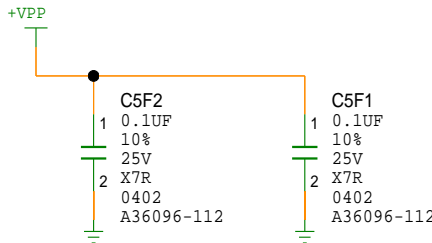
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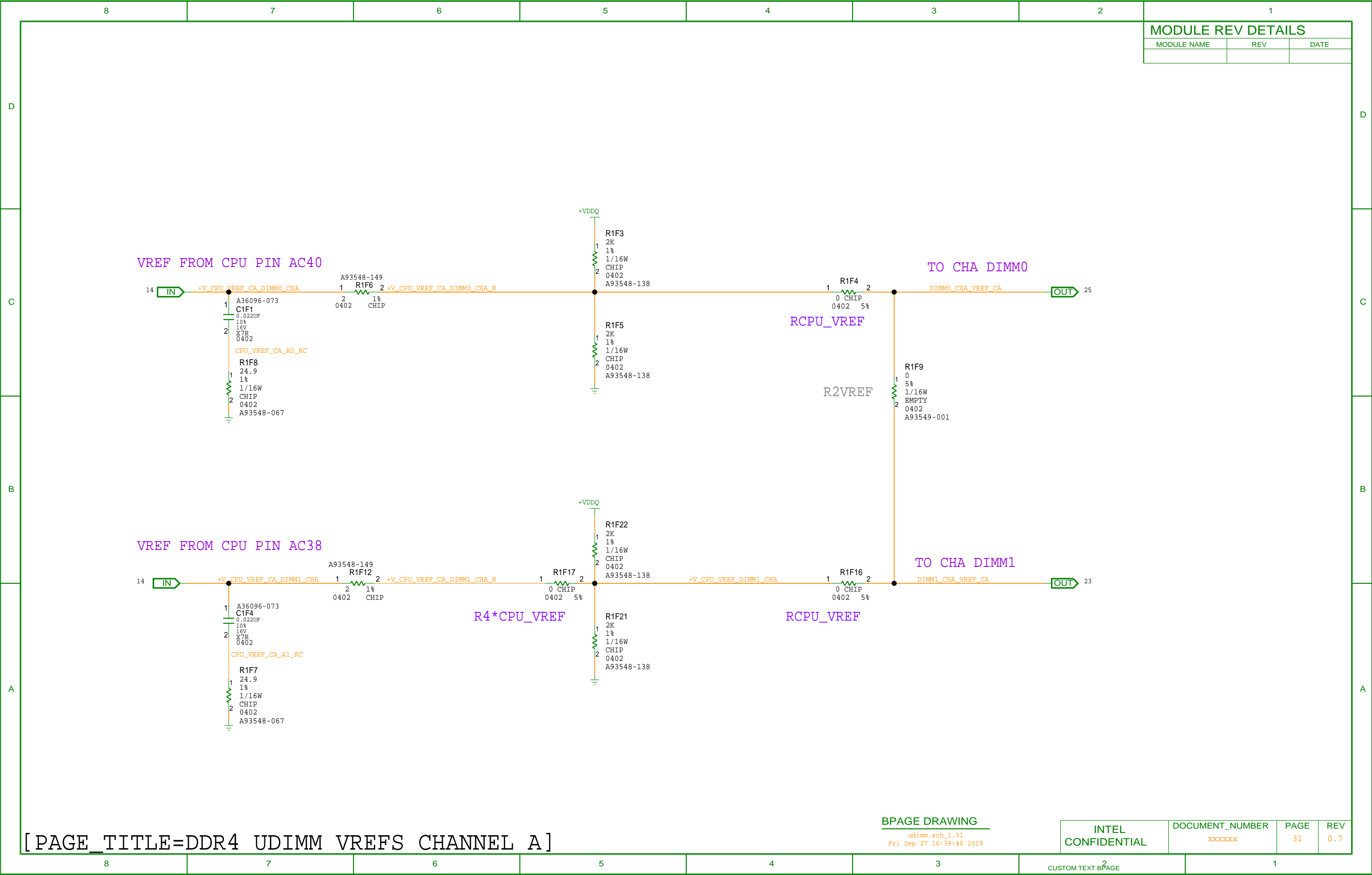
MODULE REV DETAILS

MODULE NAME	REV	DATE



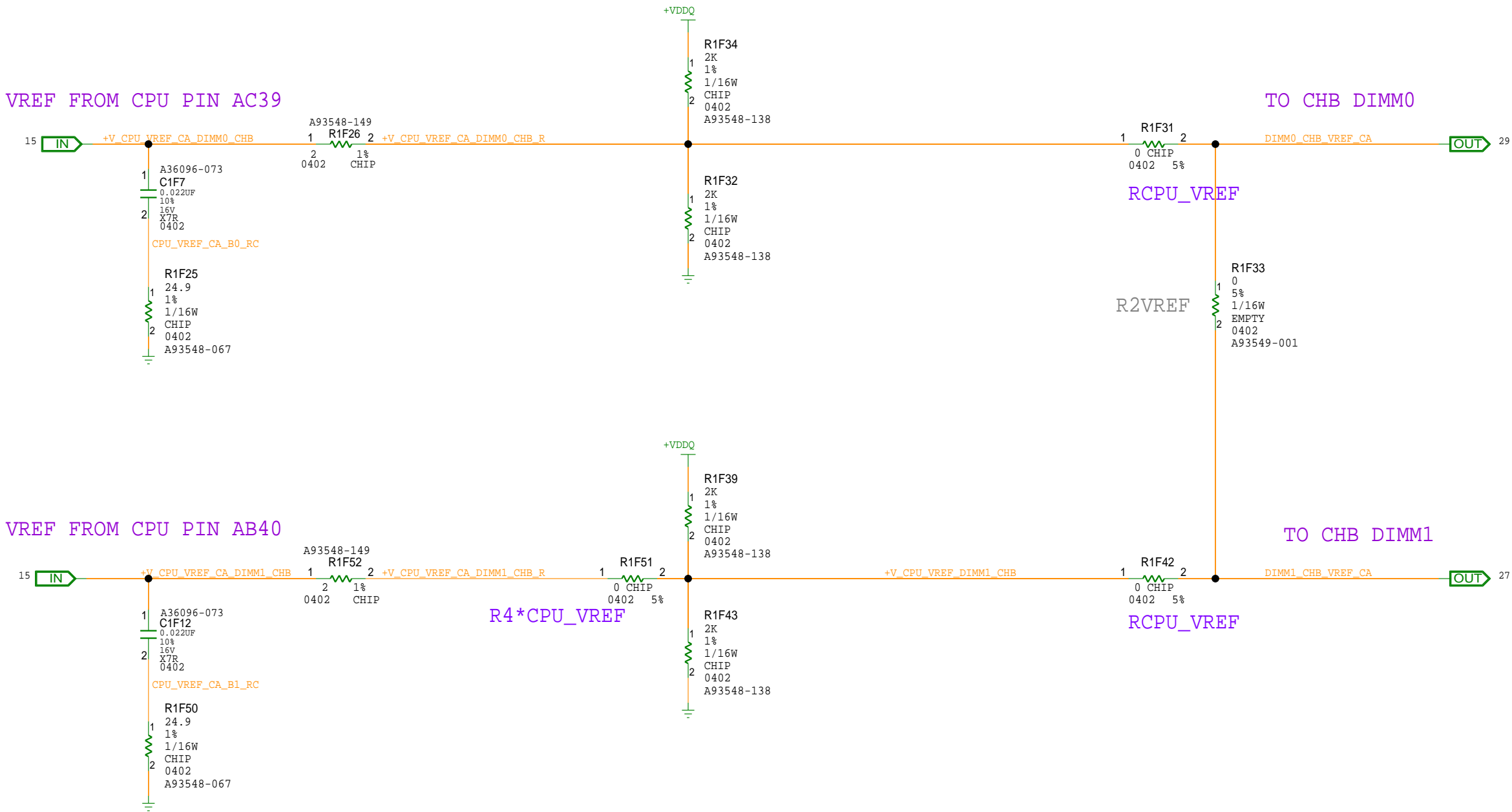
DESIGN NOTE:  
CH B VDDQ\_VTT DECOUPLING CAPS





MODULE REV DETAILS

MODULE NAME	REV	DATE

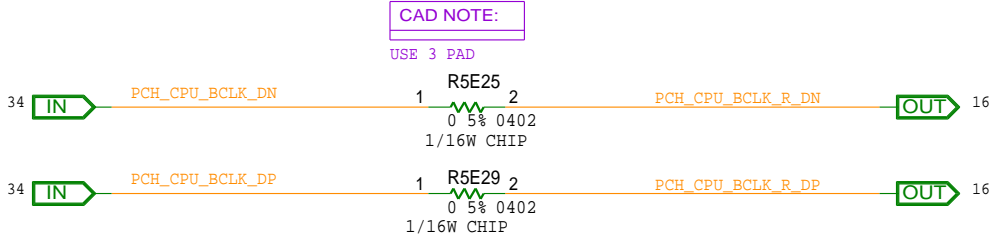


8		7		6		5		4		3		2		1			
														MODULE REV DETAILS			
														MODULE NAME		REV	DATE
D															D		
C															C		
B															B		
A															A		
[ PAGE_TITLE=BLANK ]																	
8		7		6		5		4		3		CUSTOM TEXT B		PAGE			
												INTEL CONFIDENTIAL		DOCUMENT_NUMBER	PAGE		
														xxxxxxx	33		
															REV		
															0.7		

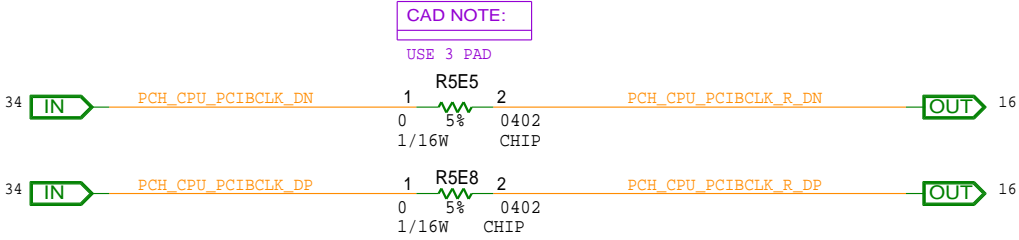




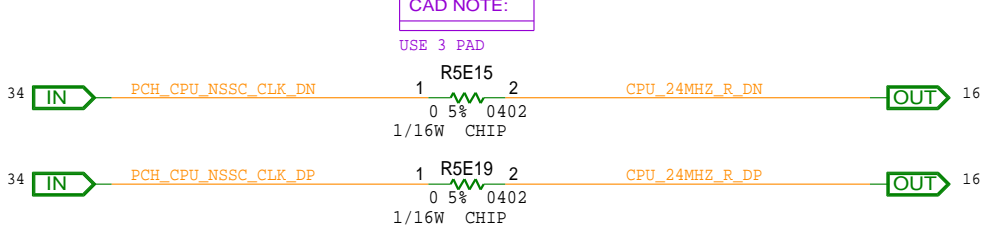
CPU BCLK OPTIONS



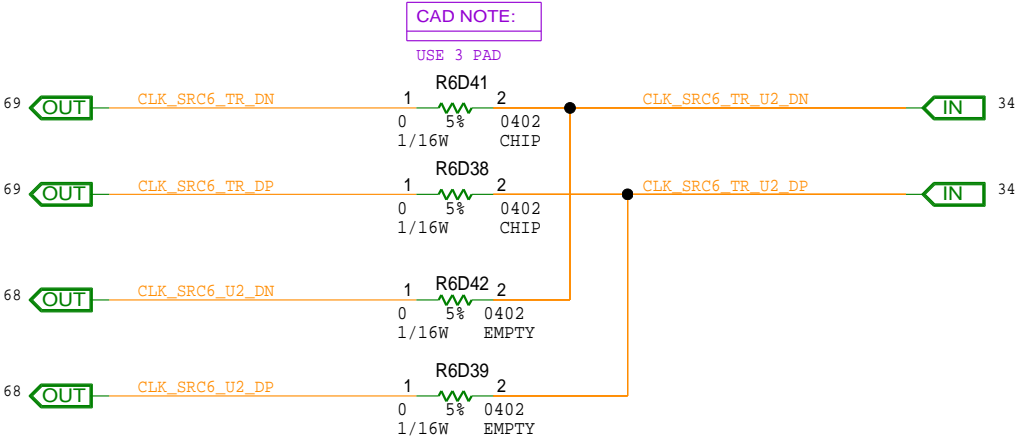
CPU PCIBCLK OPTIONS



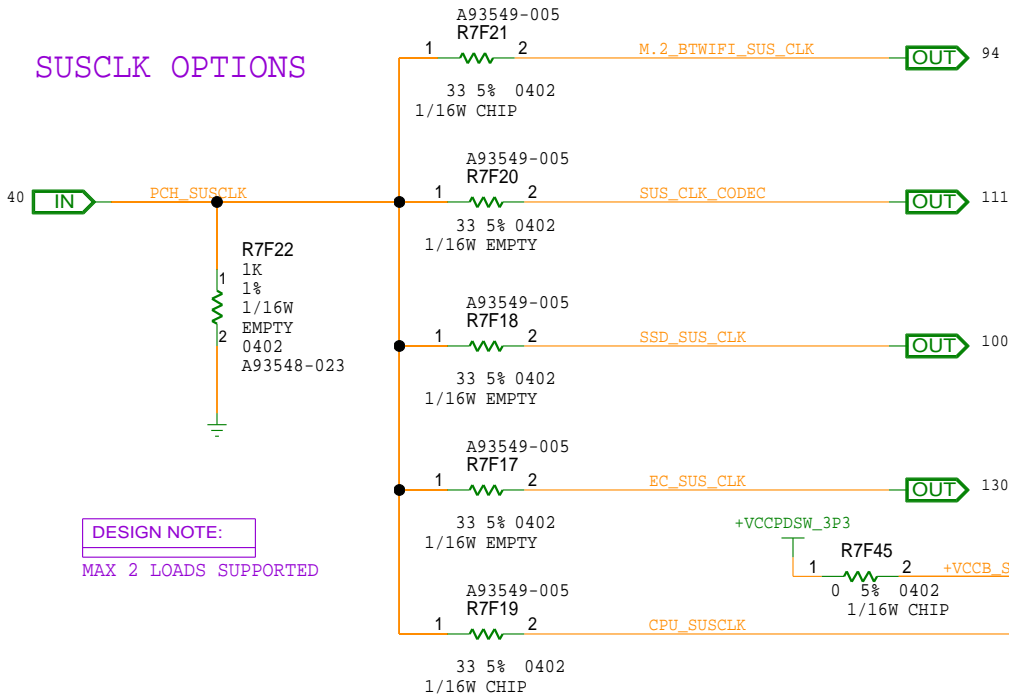
CPU NSSC CLK OPTIONS



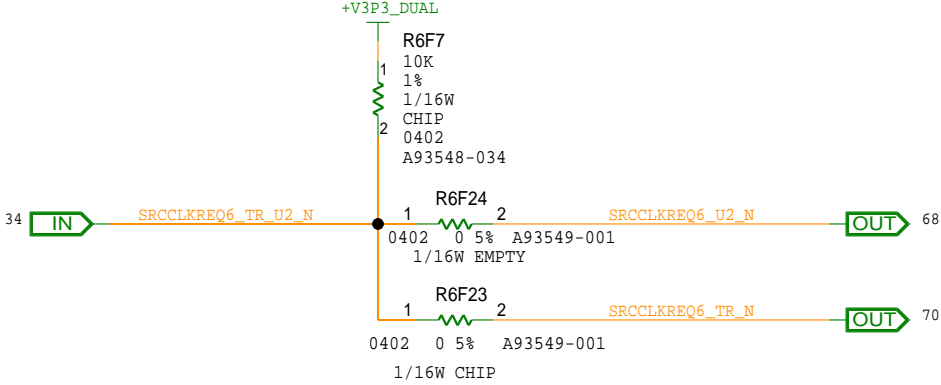
SRC FOR BP TR / FP TR(AIC VIA U.2) OPTIONS



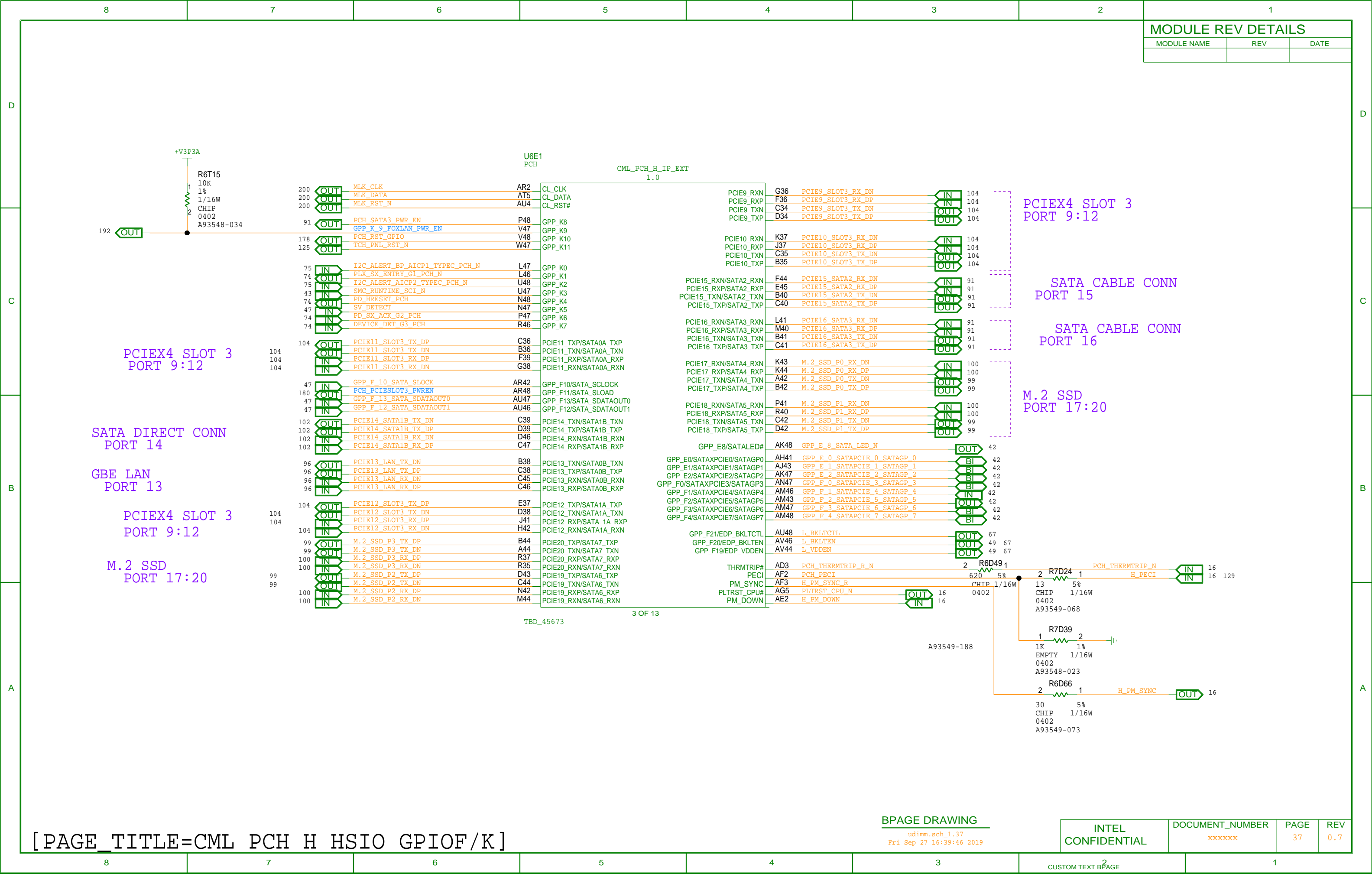
SUSCLK OPTIONS



CLKREQ# FOR BP TR / FP TR(AIC VIA U.2) OPTIONS



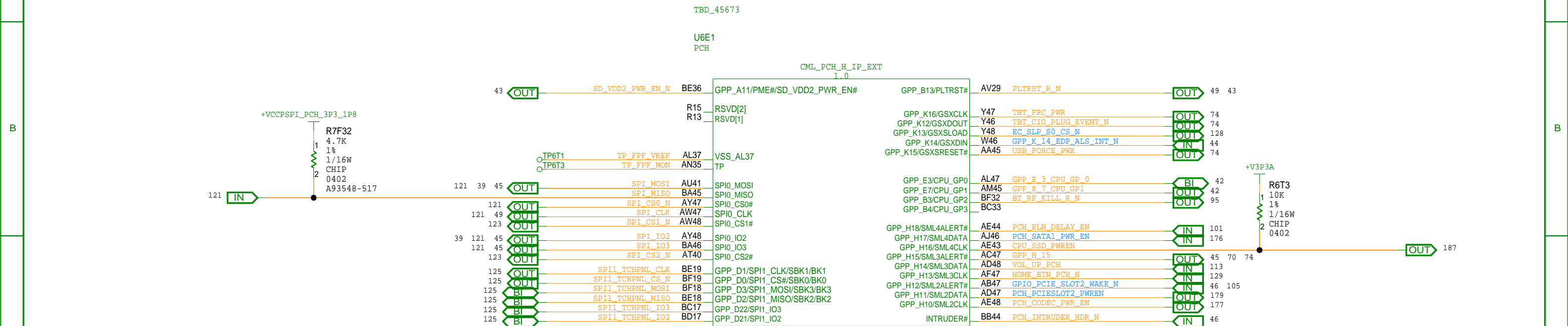
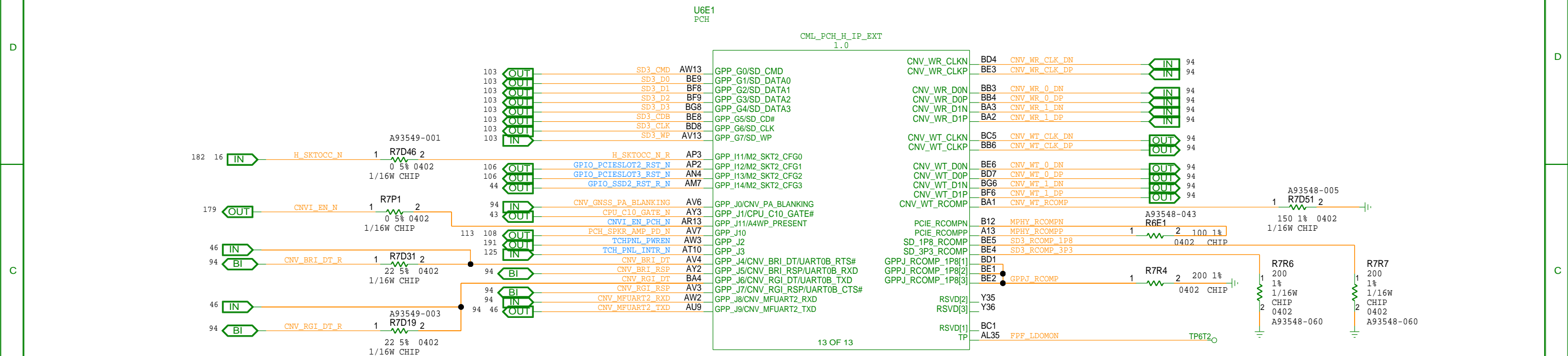
[illegible][illegible]







MODULE REV DETAILS		
MODULE NAME	REV	DATE



The diagram shows two resistors, R7F34 and R7T14, connected between XDP\_SPI0\_IO2 and XDP\_SPI0\_MOSI pins and SPI\_IO2 and SPI\_MOSI pins. Both resistors are 1K 1% 0402 1/16W CHIP.

DATE	DOCUMENT NUMBER	PAGE	REV
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[PAGE TITLE=CML PCH H CNVT SD SPT GPIOH/I/J]

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REV  
0.7

[PAGE = 111111 ONE FOR IT ONE SP SP1 SP10H/175]									
8	7	6	5	4	3	CUSTOM TEXT PAGE	1		

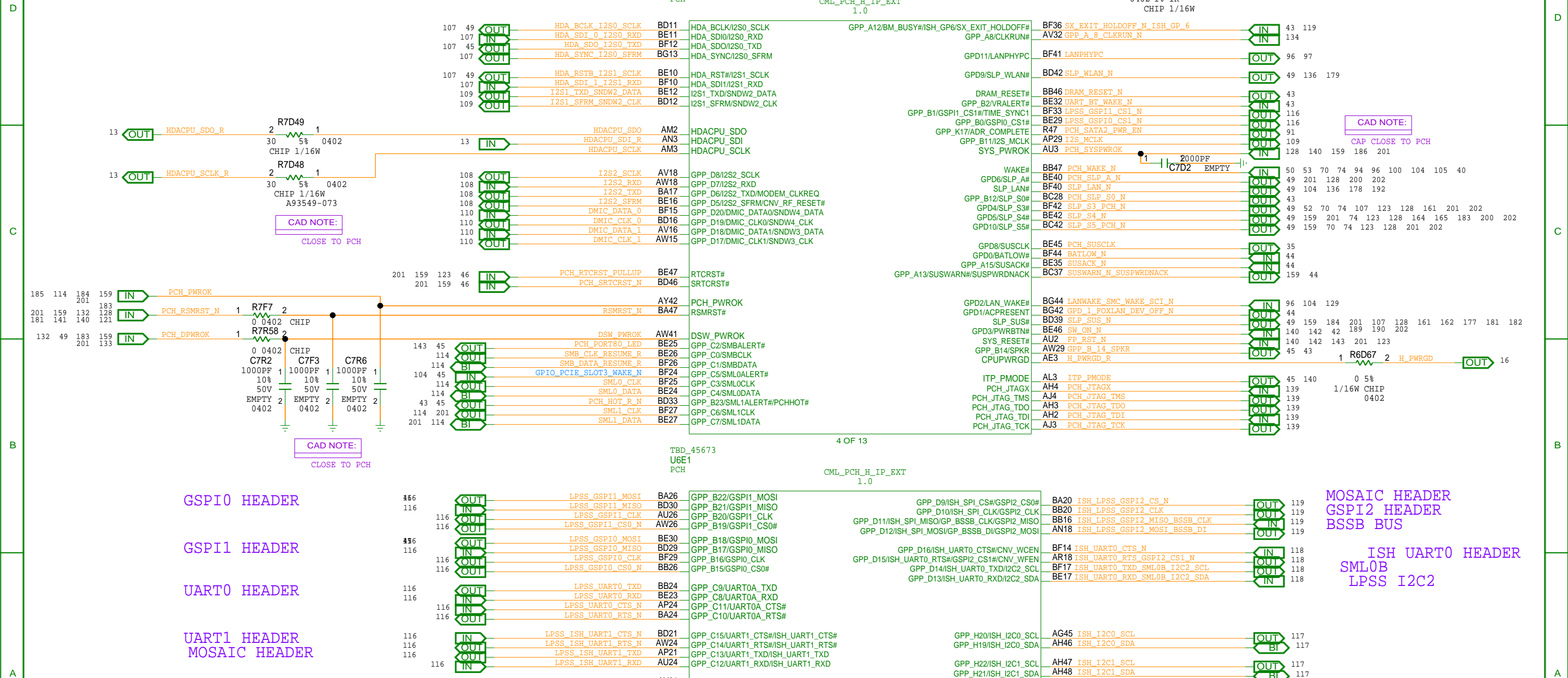
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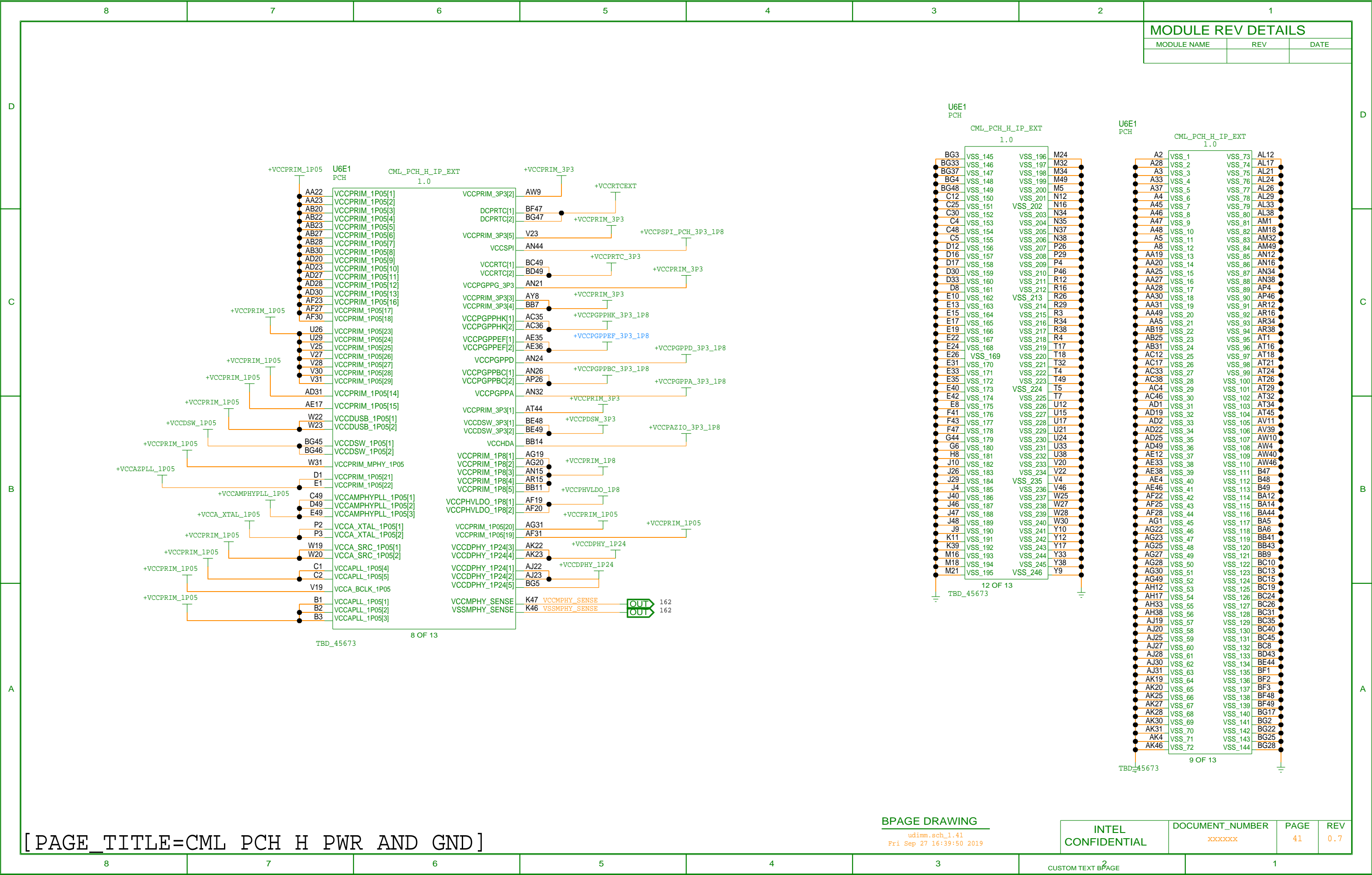
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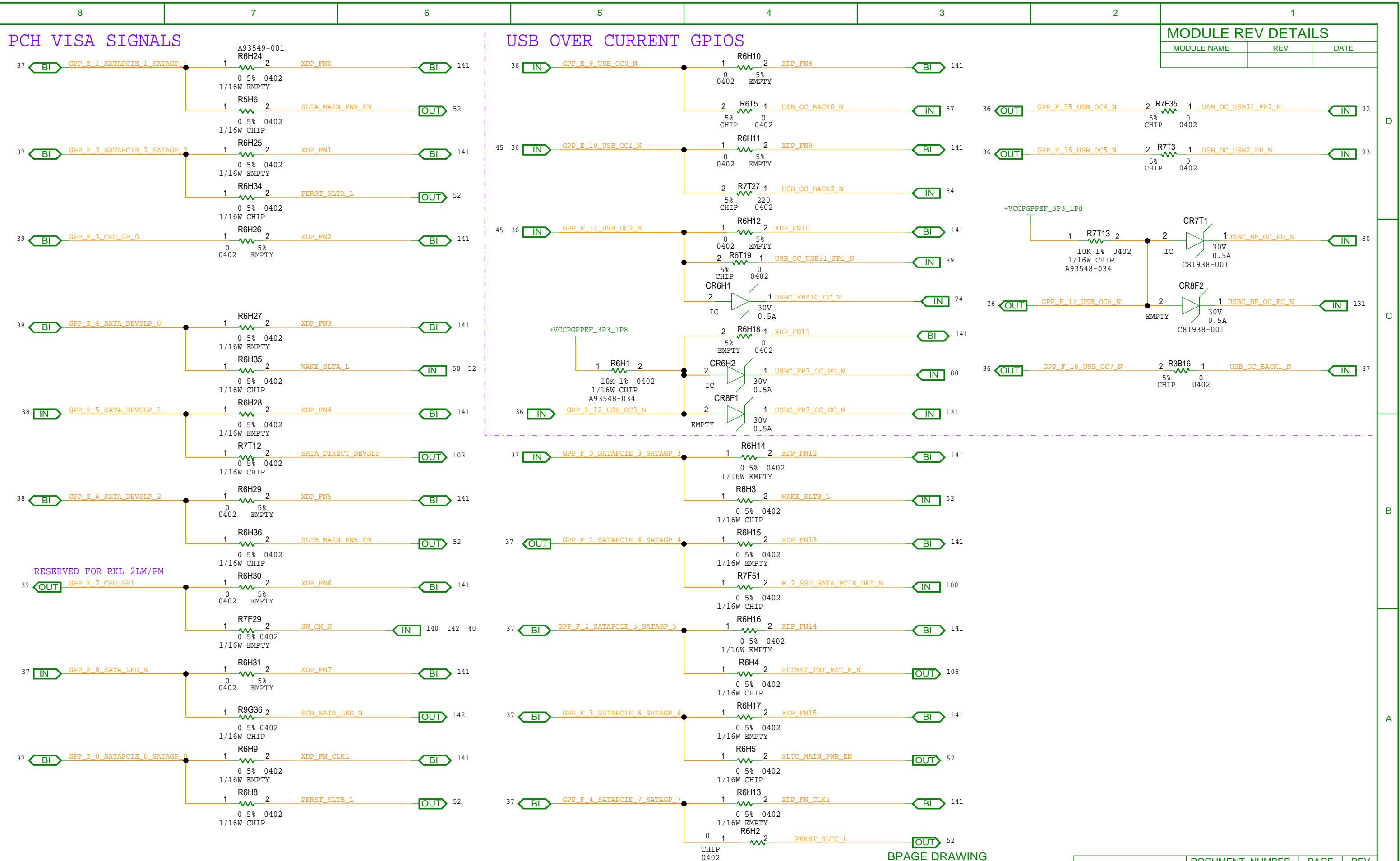
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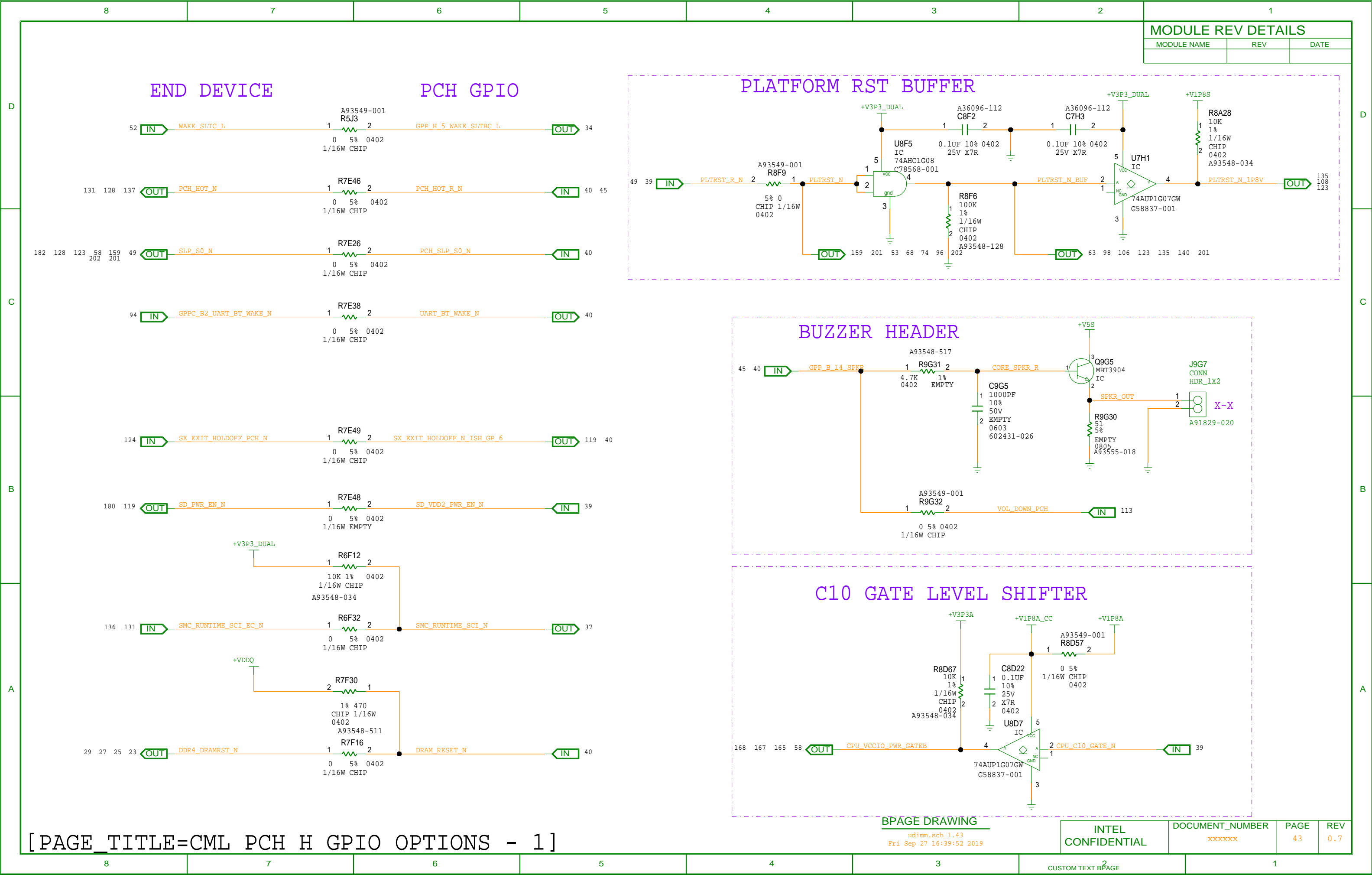
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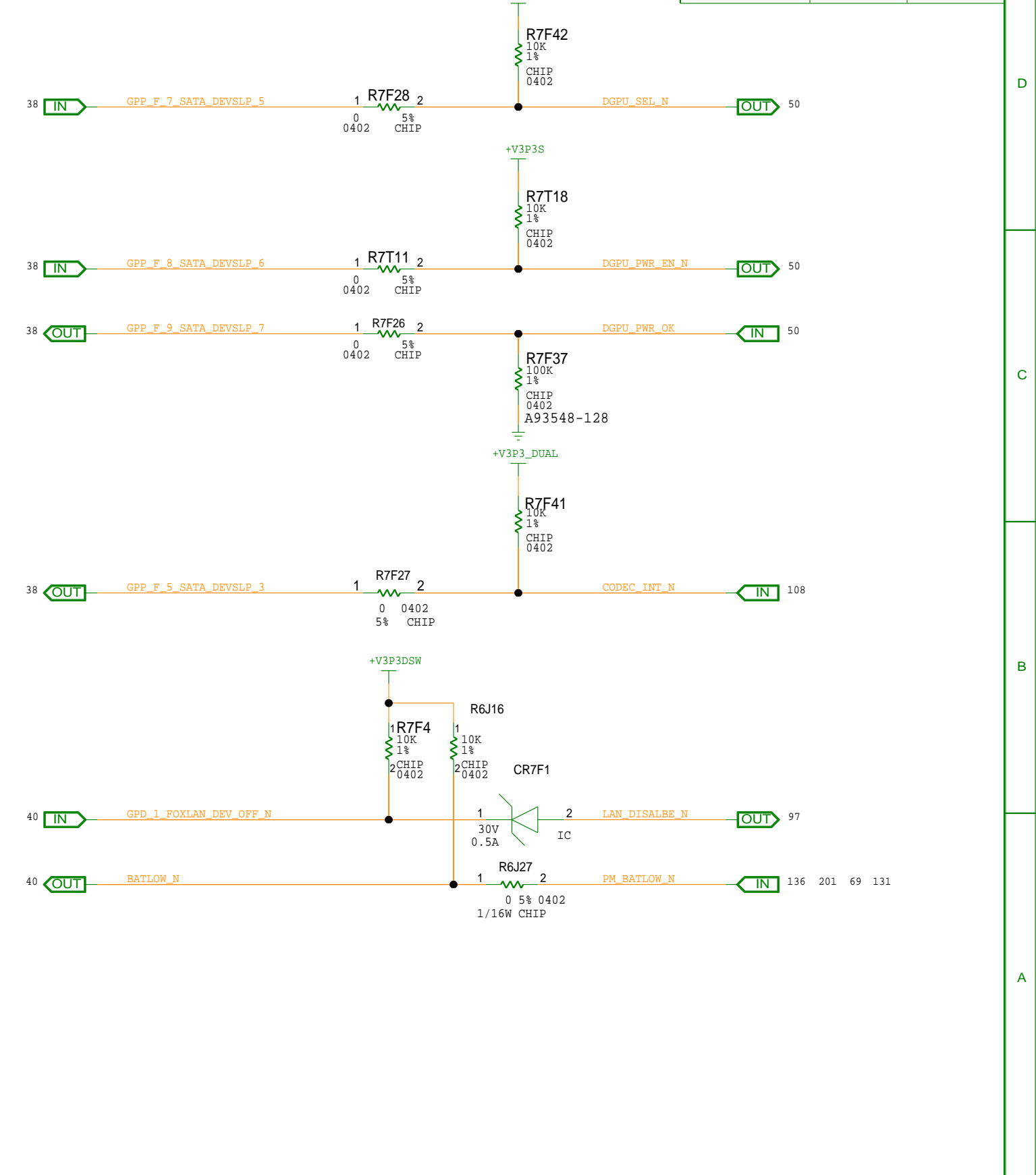
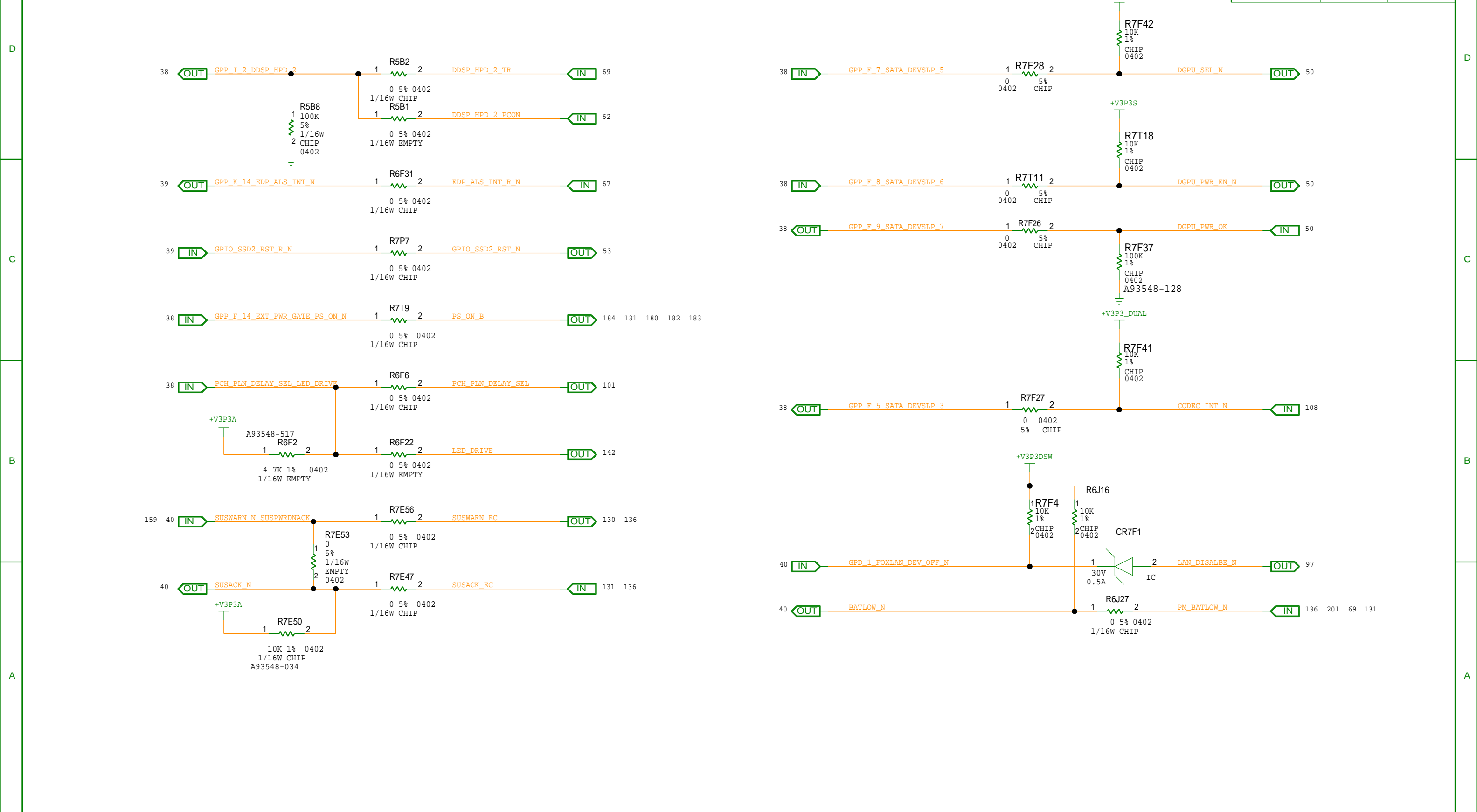








MODULE REV DETAILS		
MODULE NAME	REV	DATE



8	7	6	5	4	3	2 CUSTOM TEXT B PAGE	1
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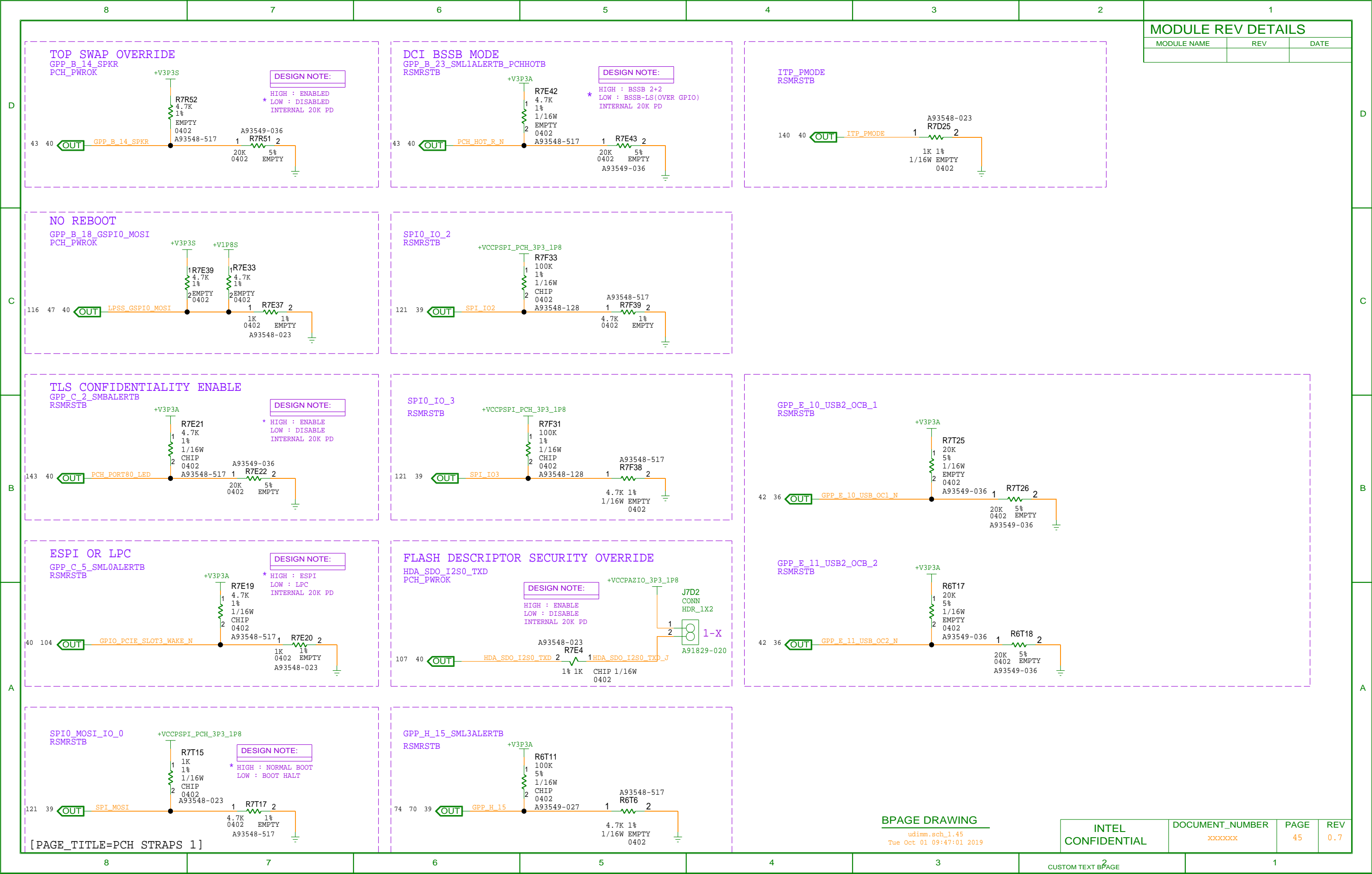
udimm.sch\_1.44  
Fri Sep 27 16:39:52 2019

CUSTOM TEXT B PAGE

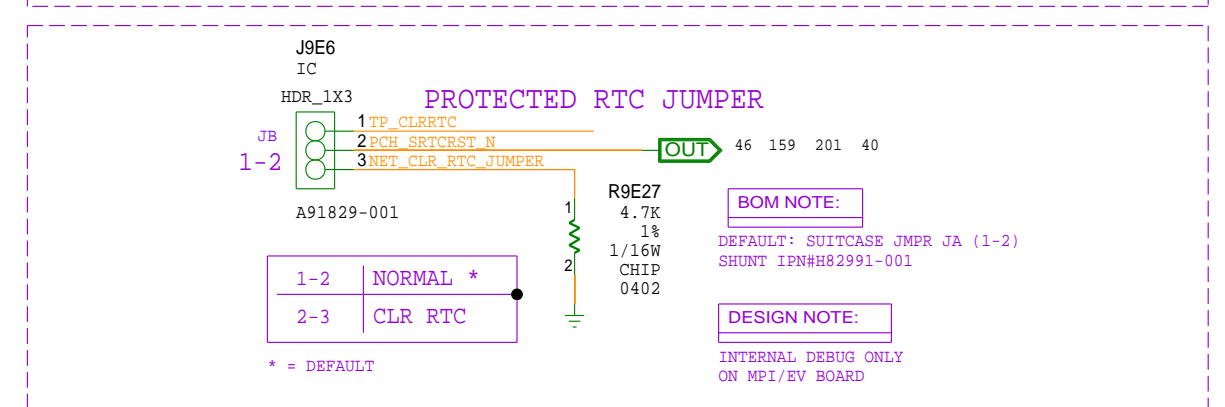
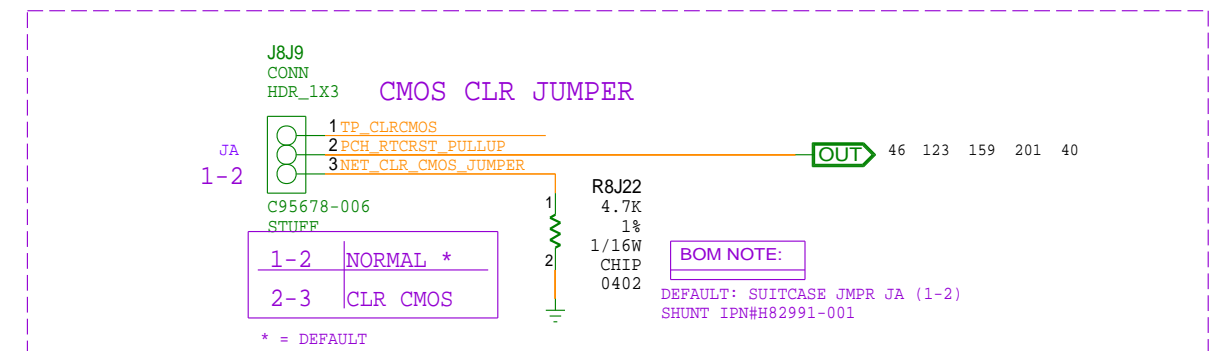
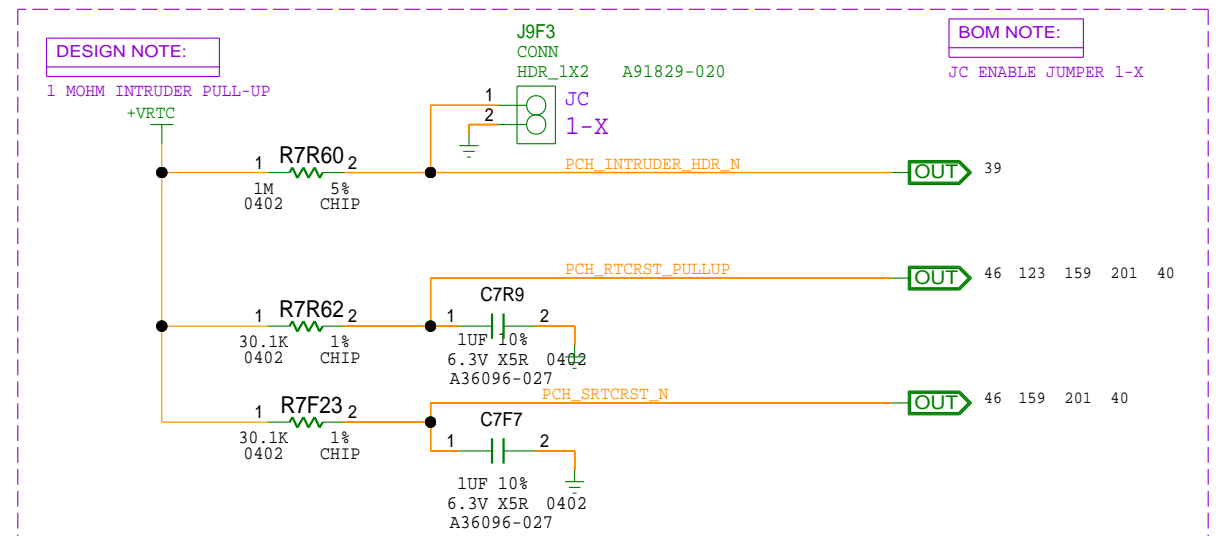
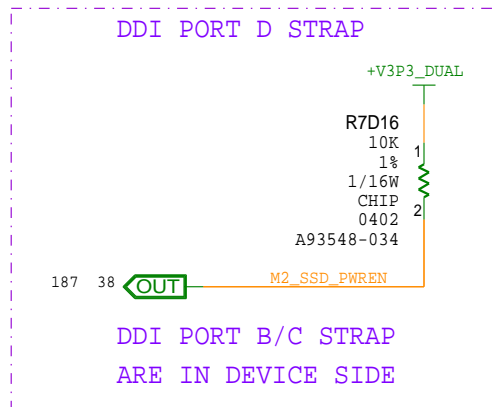
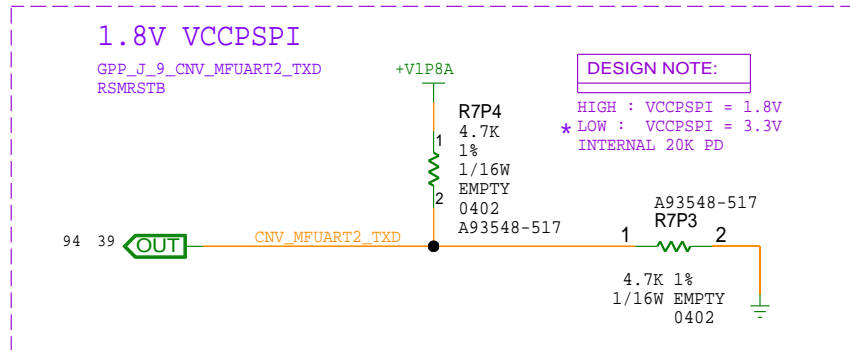
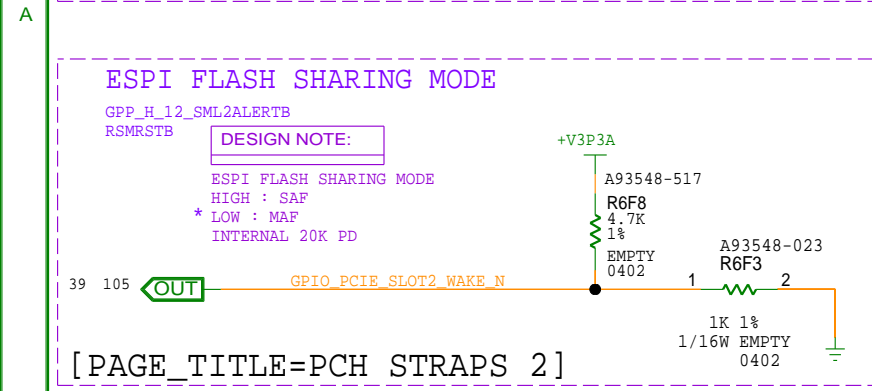
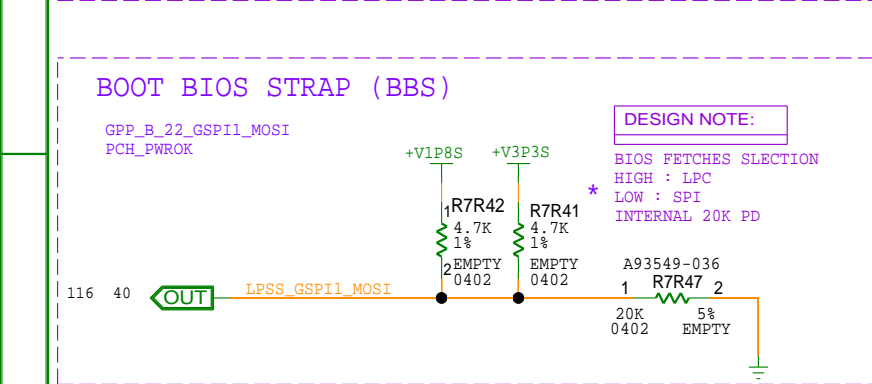
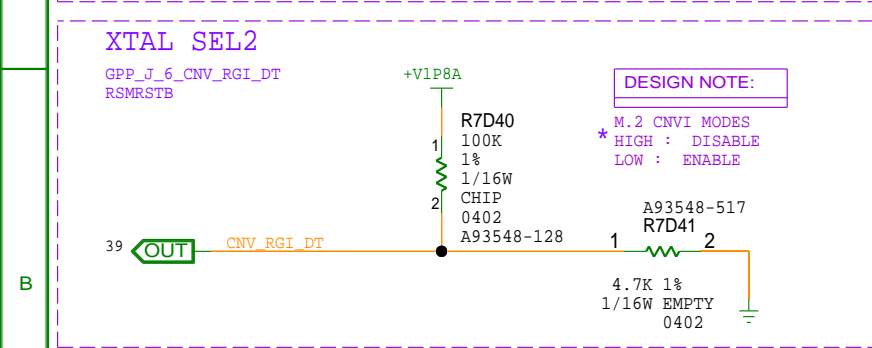
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MODULE NAME	REV	DATE



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DOCUMENT\_NUMBER

PAGE	REV
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CUSTOM TEXT B<sup>2</sup>PAGE

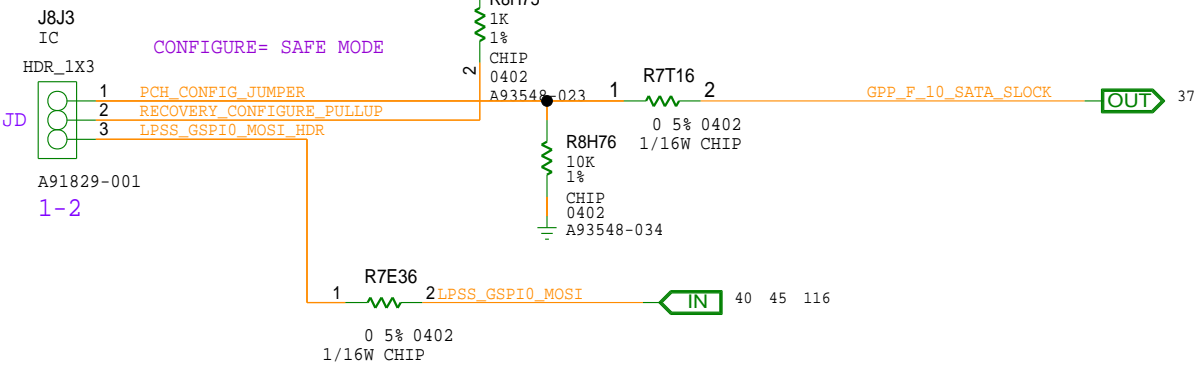
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MODULE REV DETAILS

MODULE NAME	REV	DATE

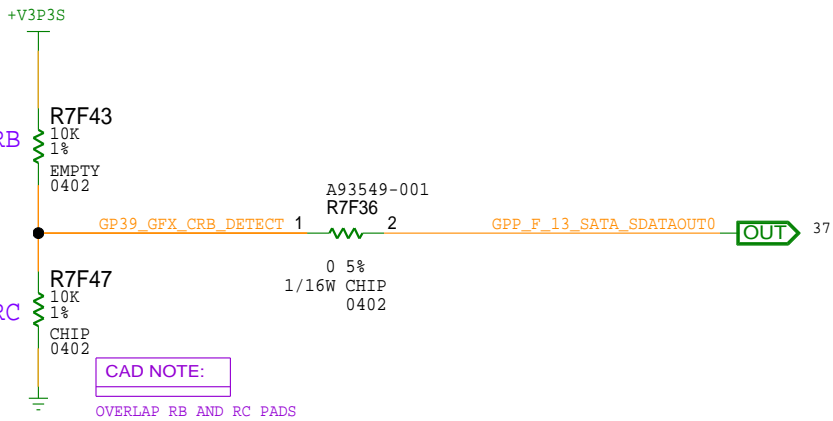
DESIGN NOTE:

FOR SOP ENABLE AND FLASH  
STUFF FOR RECOVERY USAGE ONLY



CONFIG / RECOVERY JUMPER

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

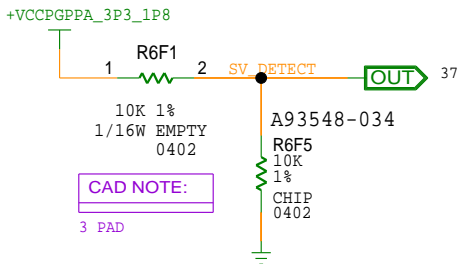


CAD NOTE:

OVERLAP RB AND RC PADS

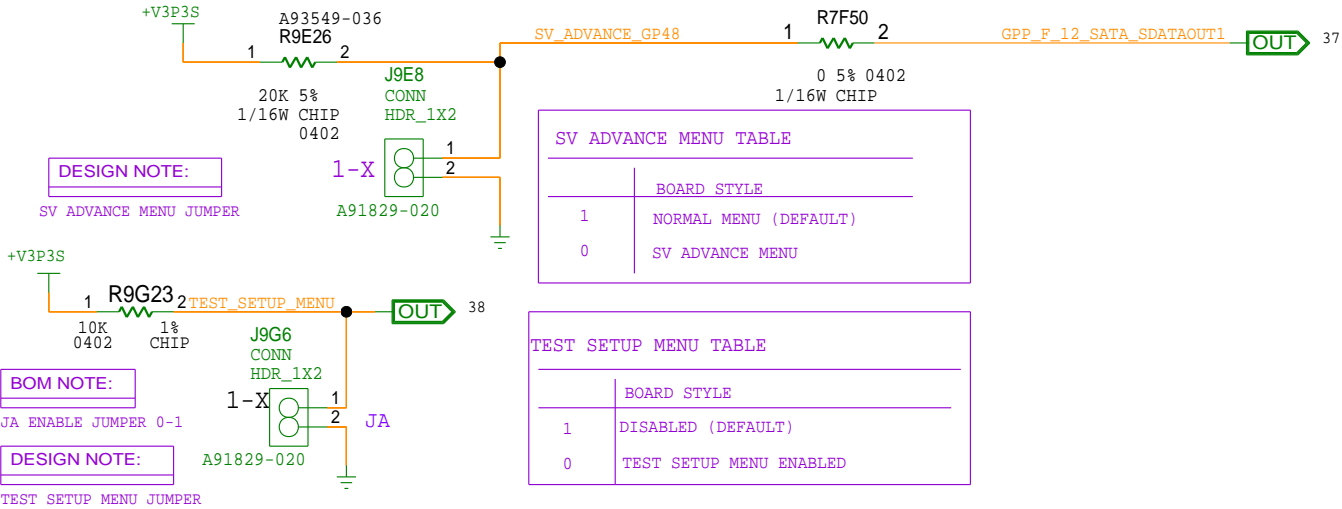
GFX SELECT TABLE

	GFX STYLE
0	NORMAL GFX
1	CUSTOMER GFX



CAD NOTE:

3 PAD



DESIGN NOTE:

SV ADVANCE MENU JUMPER

BOM NOTE:

JA ENABLE JUMPER 0-1

DESIGN NOTE:

TEST SETUP MENU JUMPER

SV ADVANCE MENU TABLE

	BOARD STYLE
1	NORMAL MENU (DEFAULT)
0	SV ADVANCE MENU

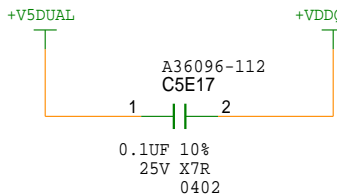
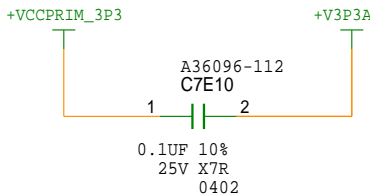
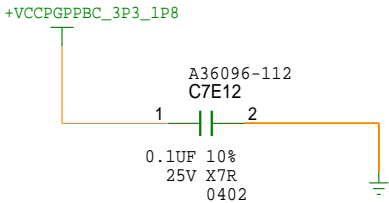
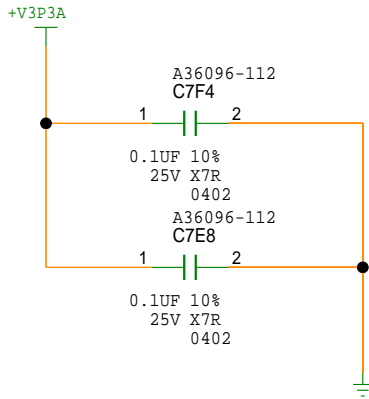
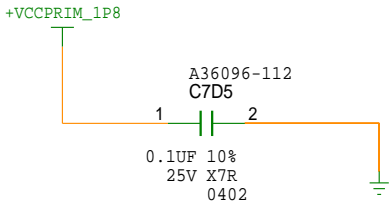
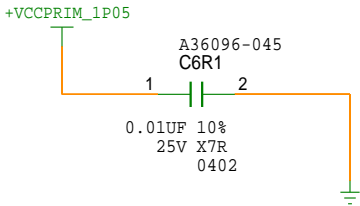
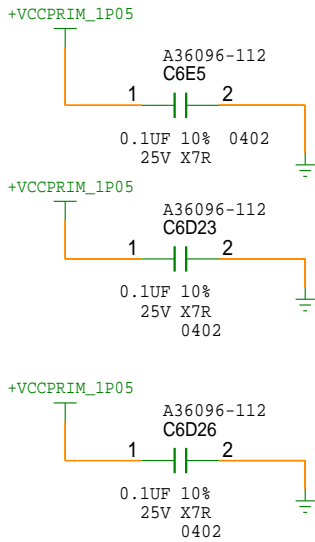
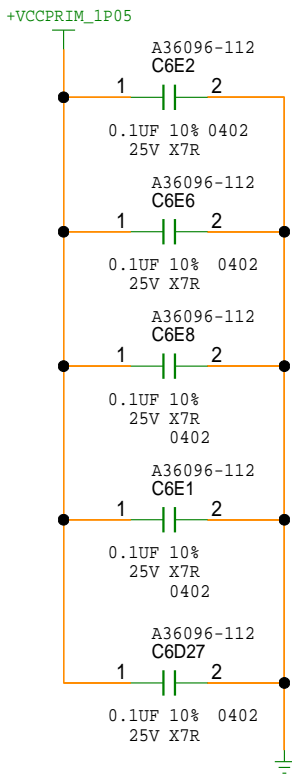
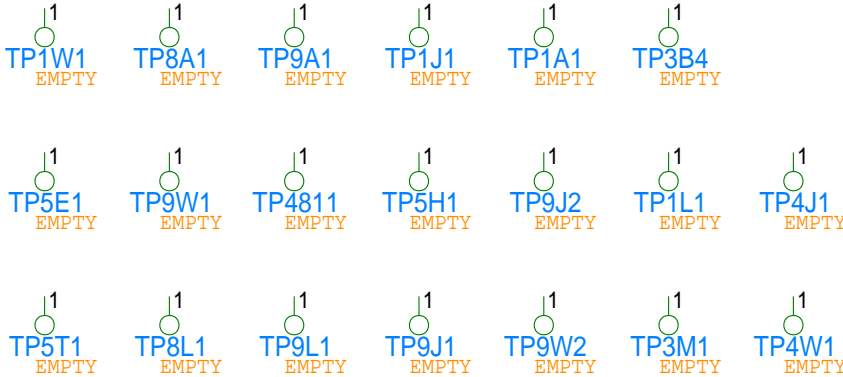
TEST SETUP MENU TABLE

	BOARD STYLE
1	DISABLED (DEFAULT)
0	TEST SETUP MENU ENABLED

MODULE REV DETAILS

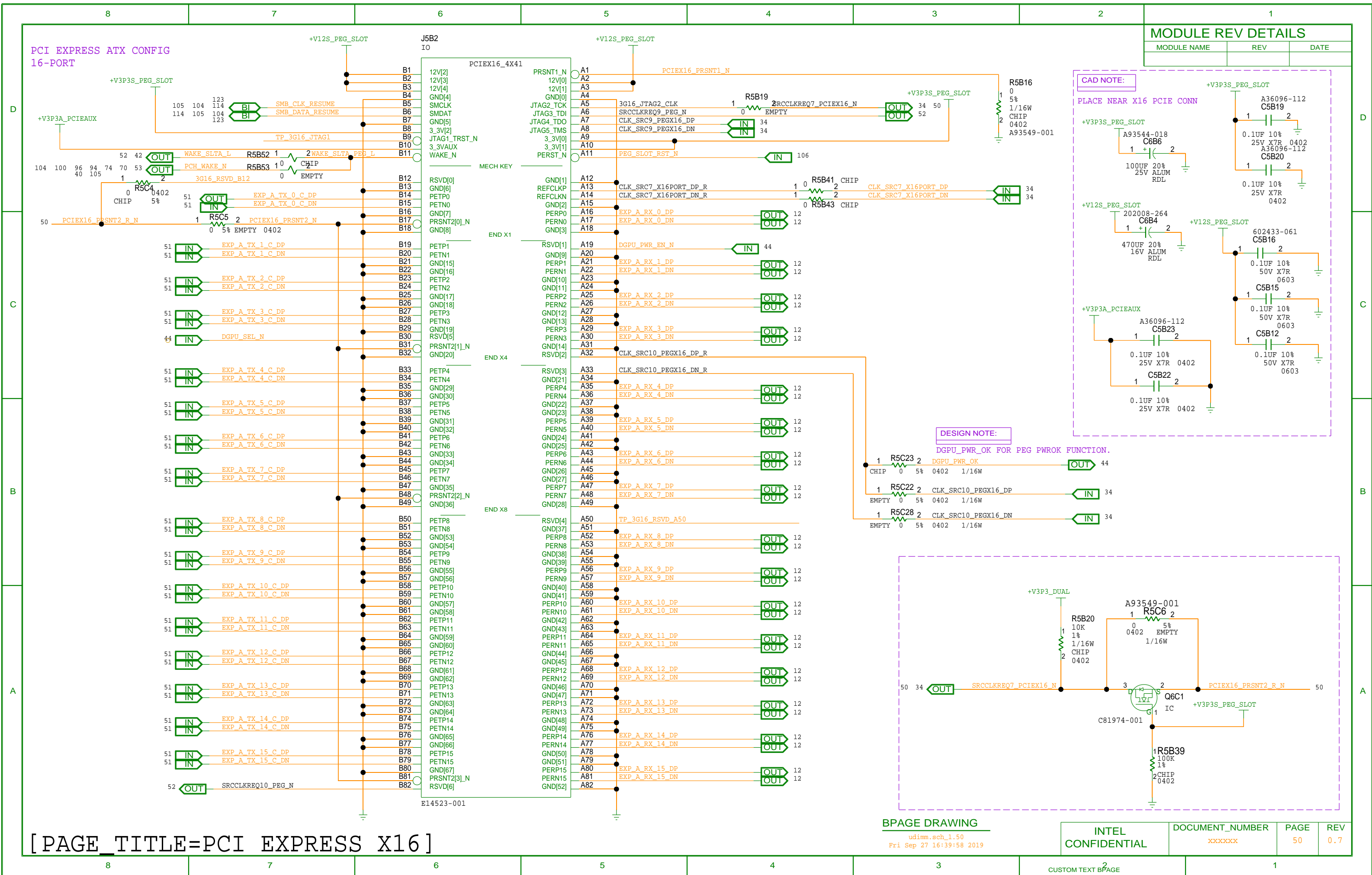
MODULE NAME	REV	DATE

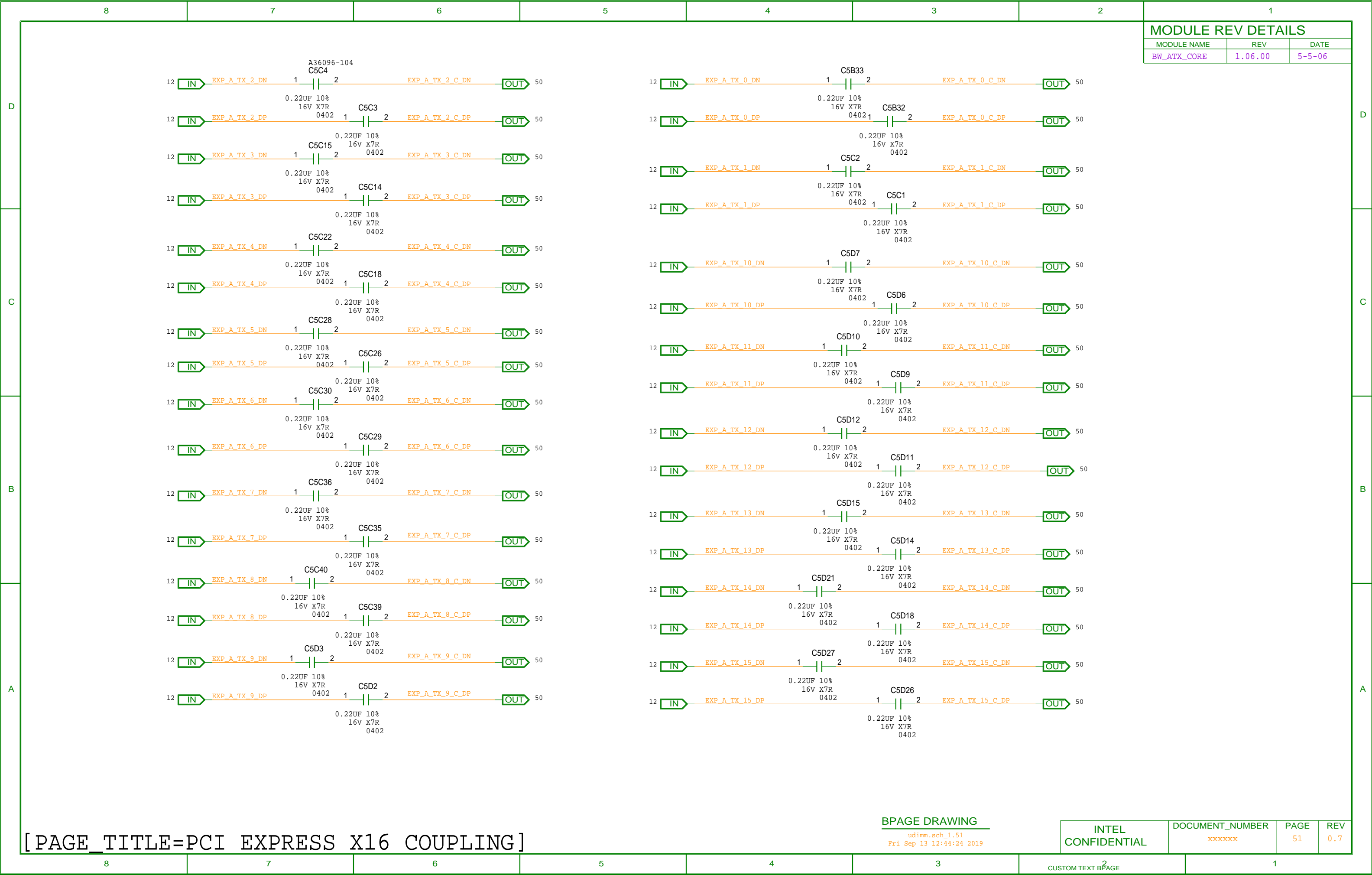
FIDUCIAL SYMBOLS ADDED AS PER GIGABYTE'S REQUEST









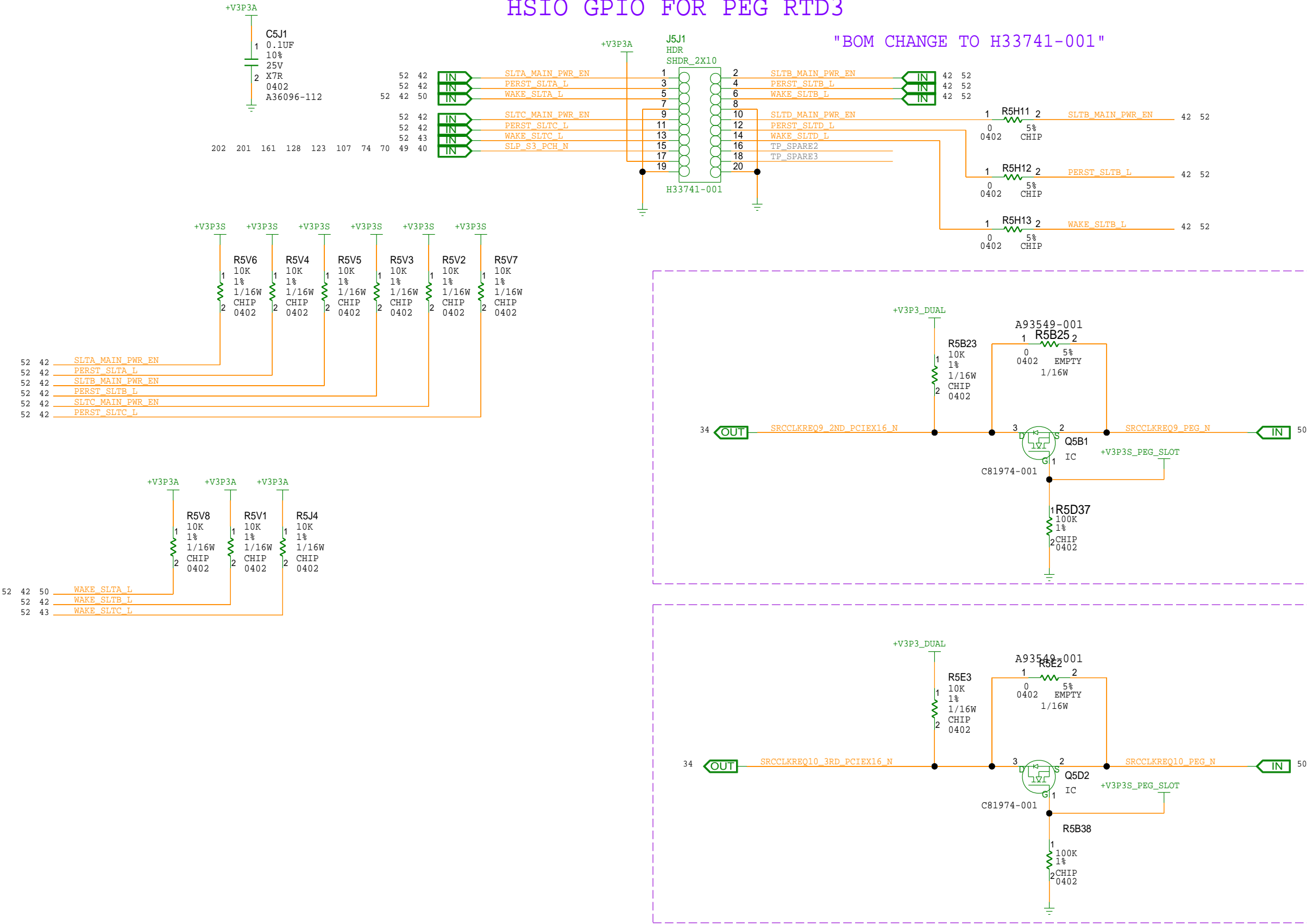


MODULE REV DETAILS

MODULE NAME	REV	DATE

HSIO GPIO FOR PEG RTD3

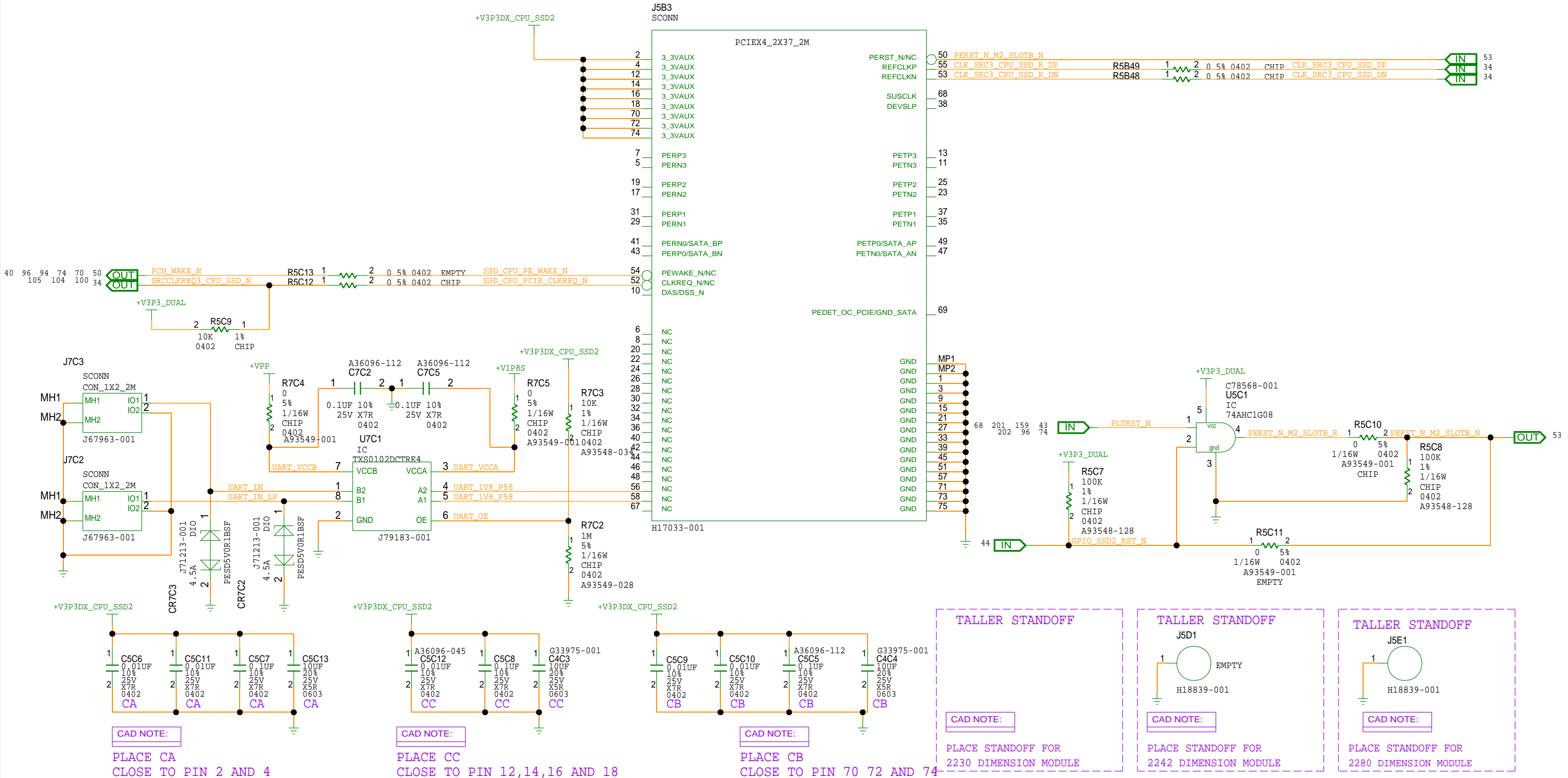
"BOM CHANGE TO H33741-001"



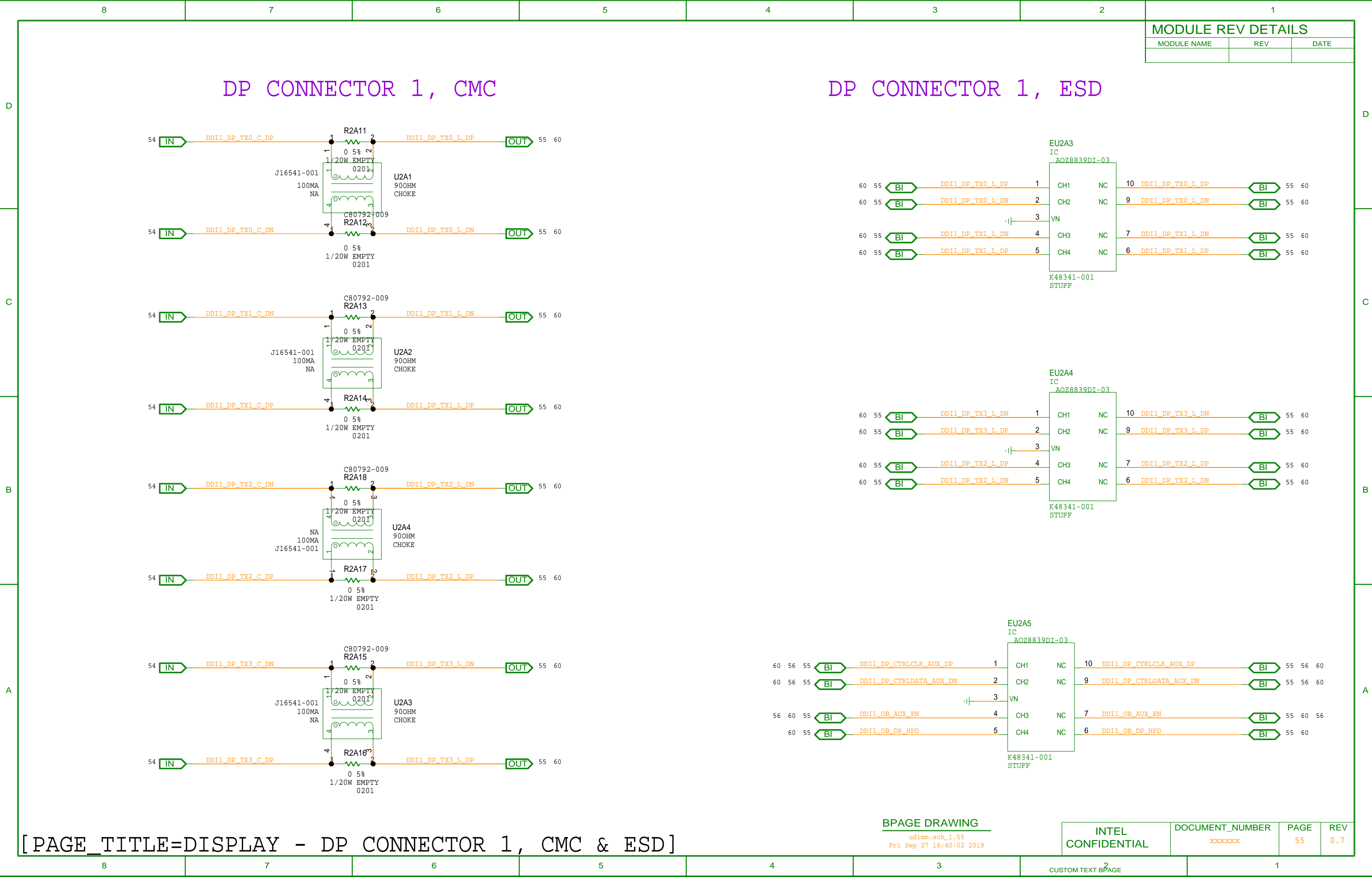
MODULE REV DETAILS

MODULE NAME	REV	DATE

M.2 X4 CONNECTOR  
8.2MM HEIGHT CONNECTOR





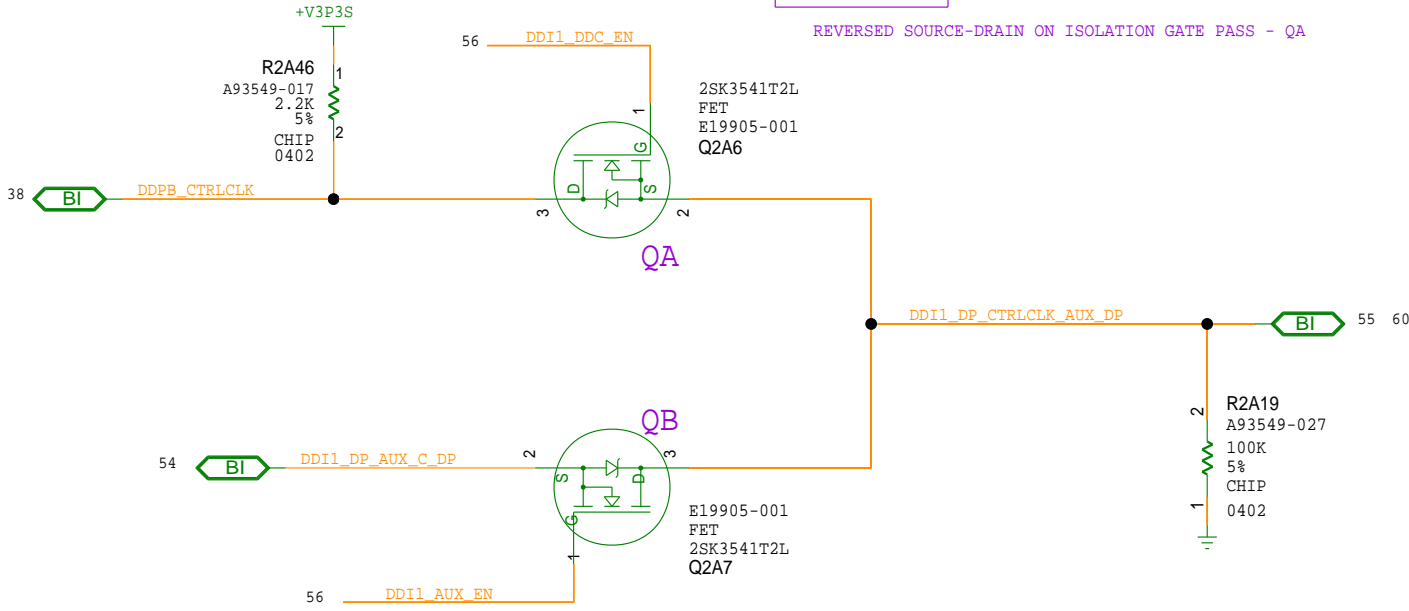


MODULE REV DETAILS

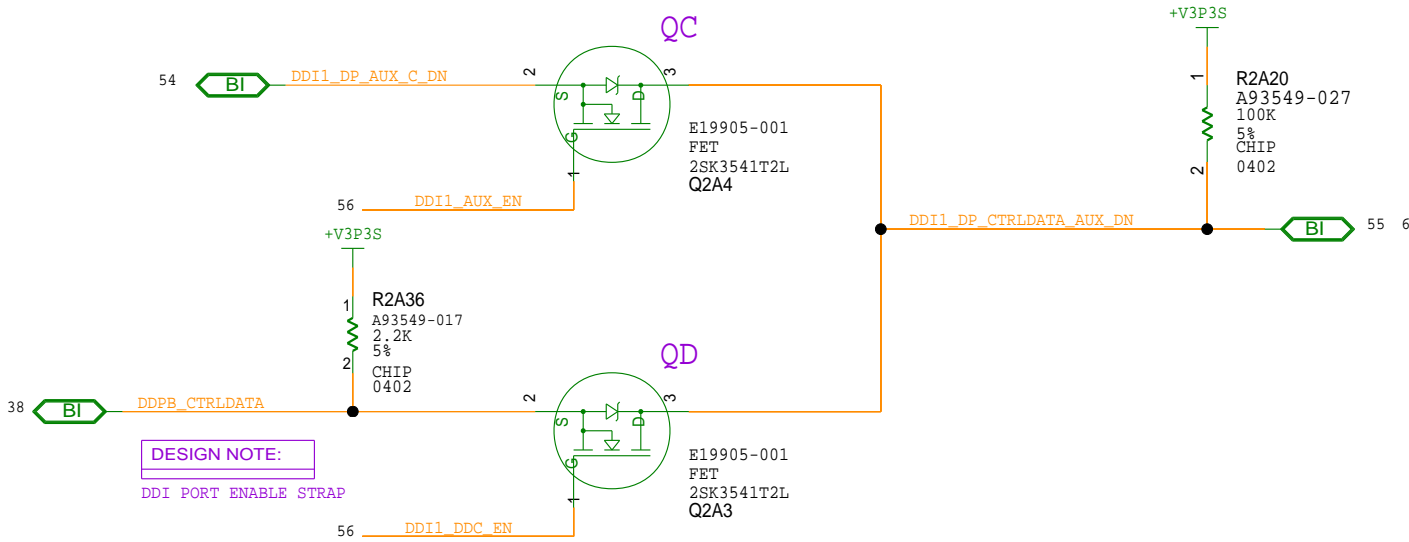
MODULE NAME	REV	DATE

DESIGN NOTE:

REVERSED SOURCE-DRAIN ON ISOLATION GATE PASS - QA



QA,QB,QC,QD: VGSTH < 1.5V

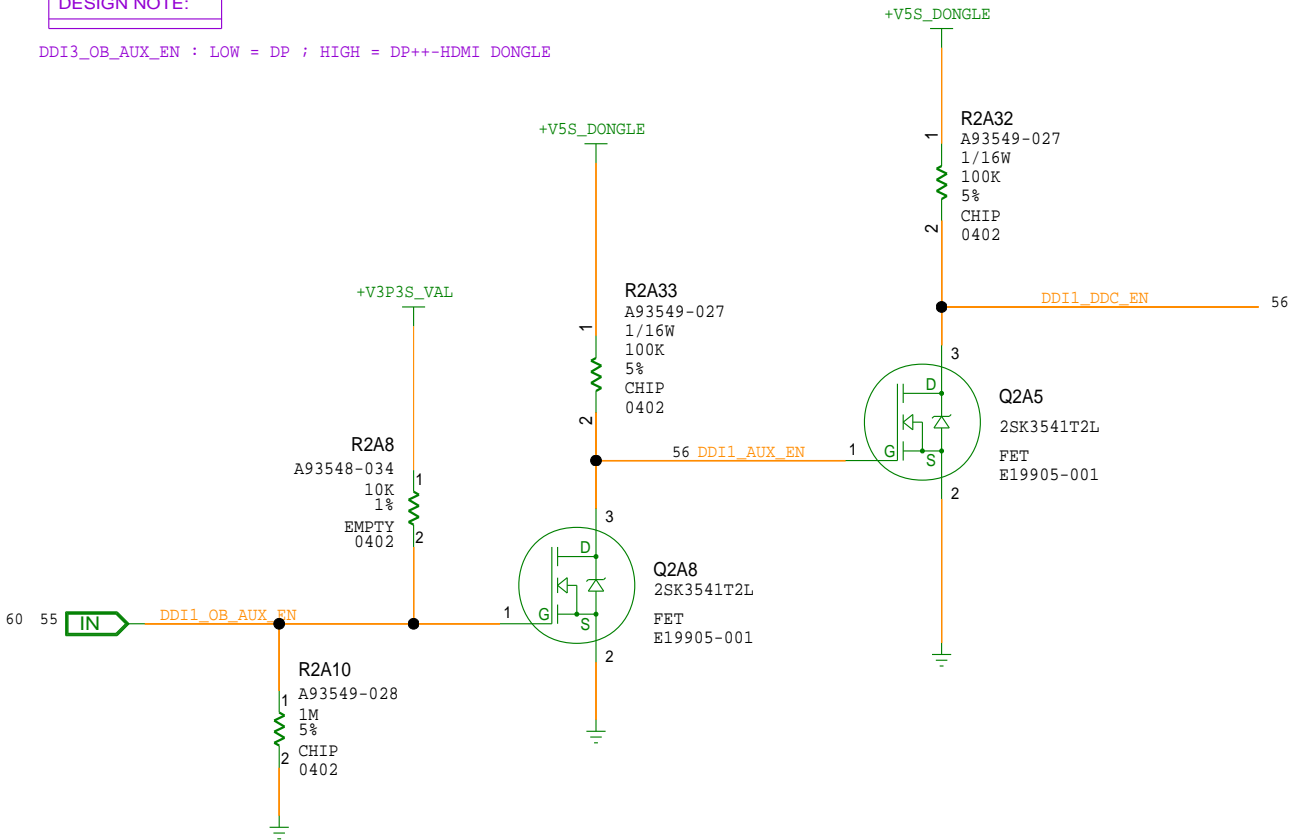


DESIGN NOTE:

DDI PORT ENABLE STRAP

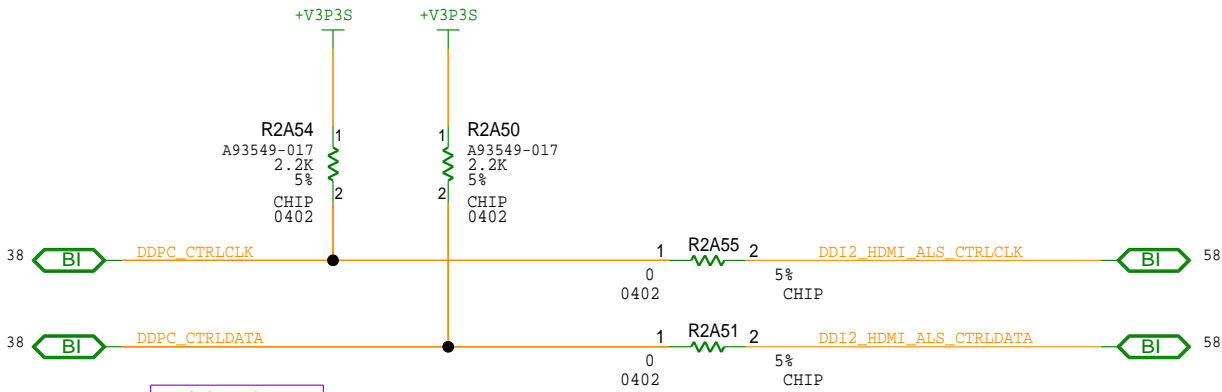
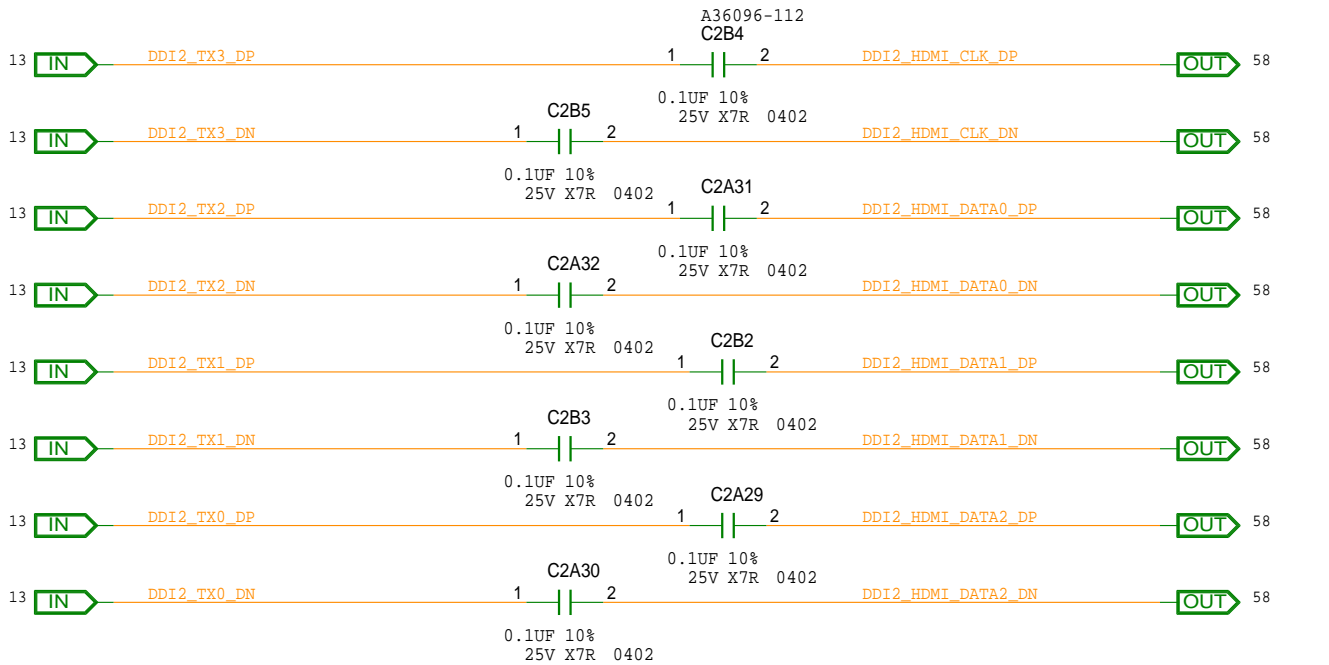
DESIGN NOTE:

DDI3\_OB\_AUX\_EN : LOW = DP ; HIGH = DP++-HDMI DONGLE



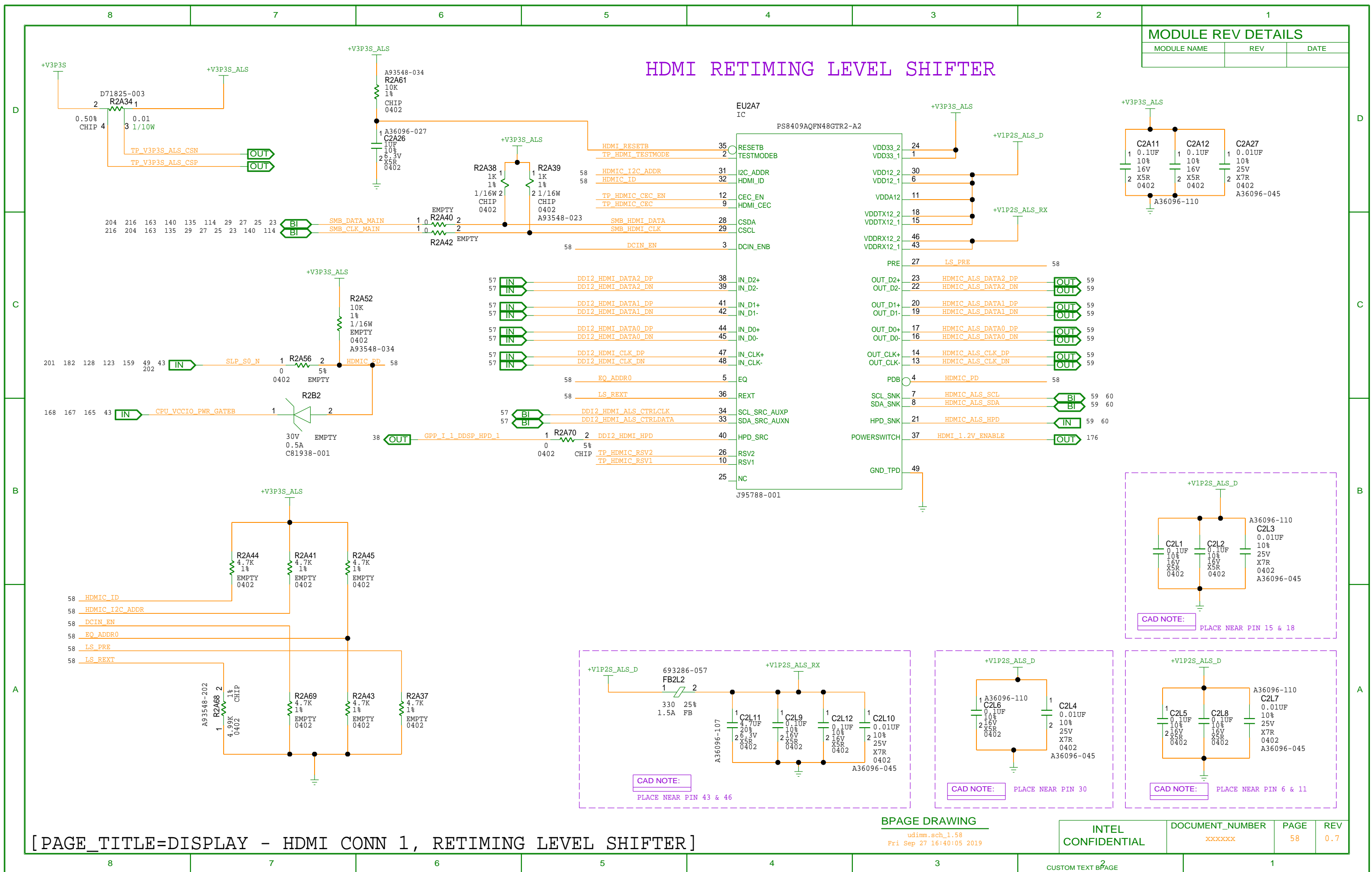
MODULE REV DETAILS

MODULE NAME	REV	DATE

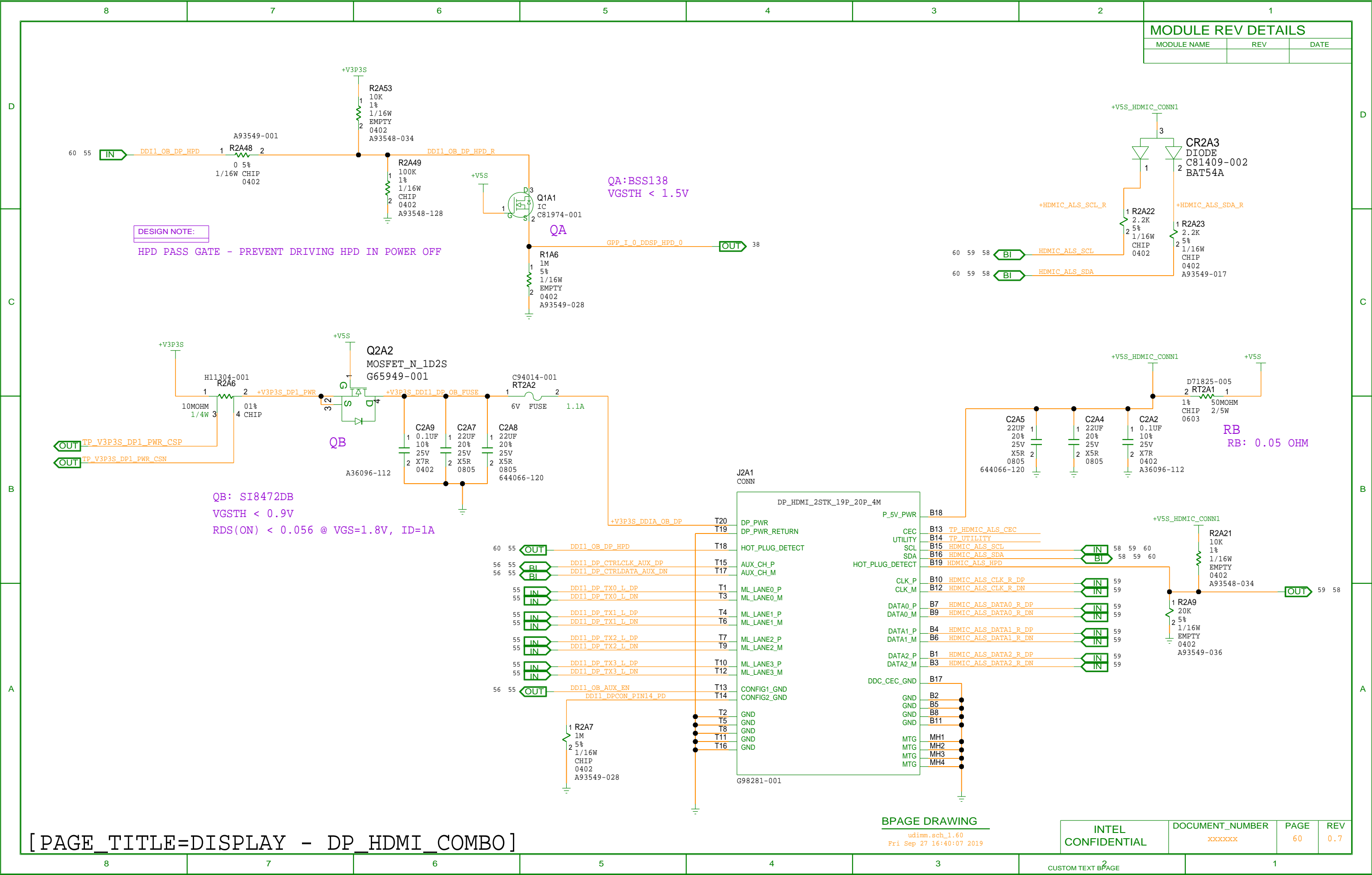


DESIGN NOTE:  
DDI PORT ENABLE STRAP

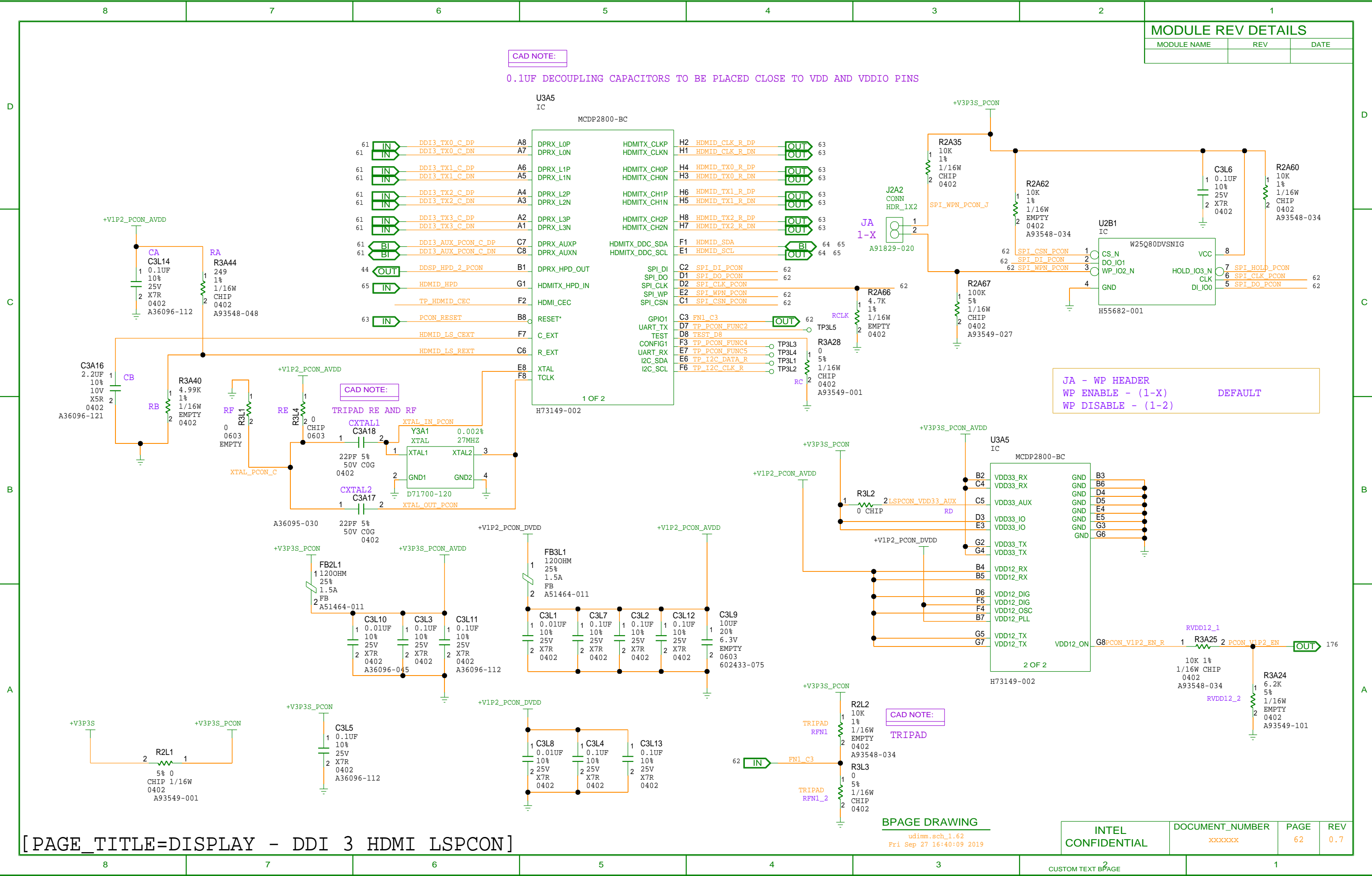












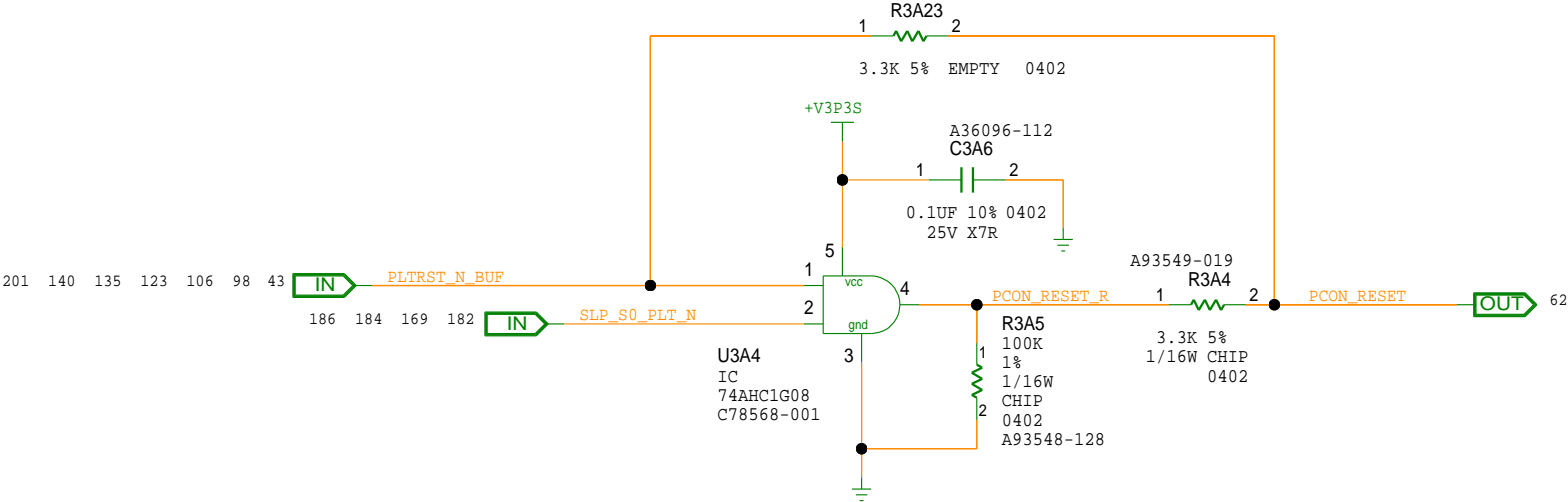
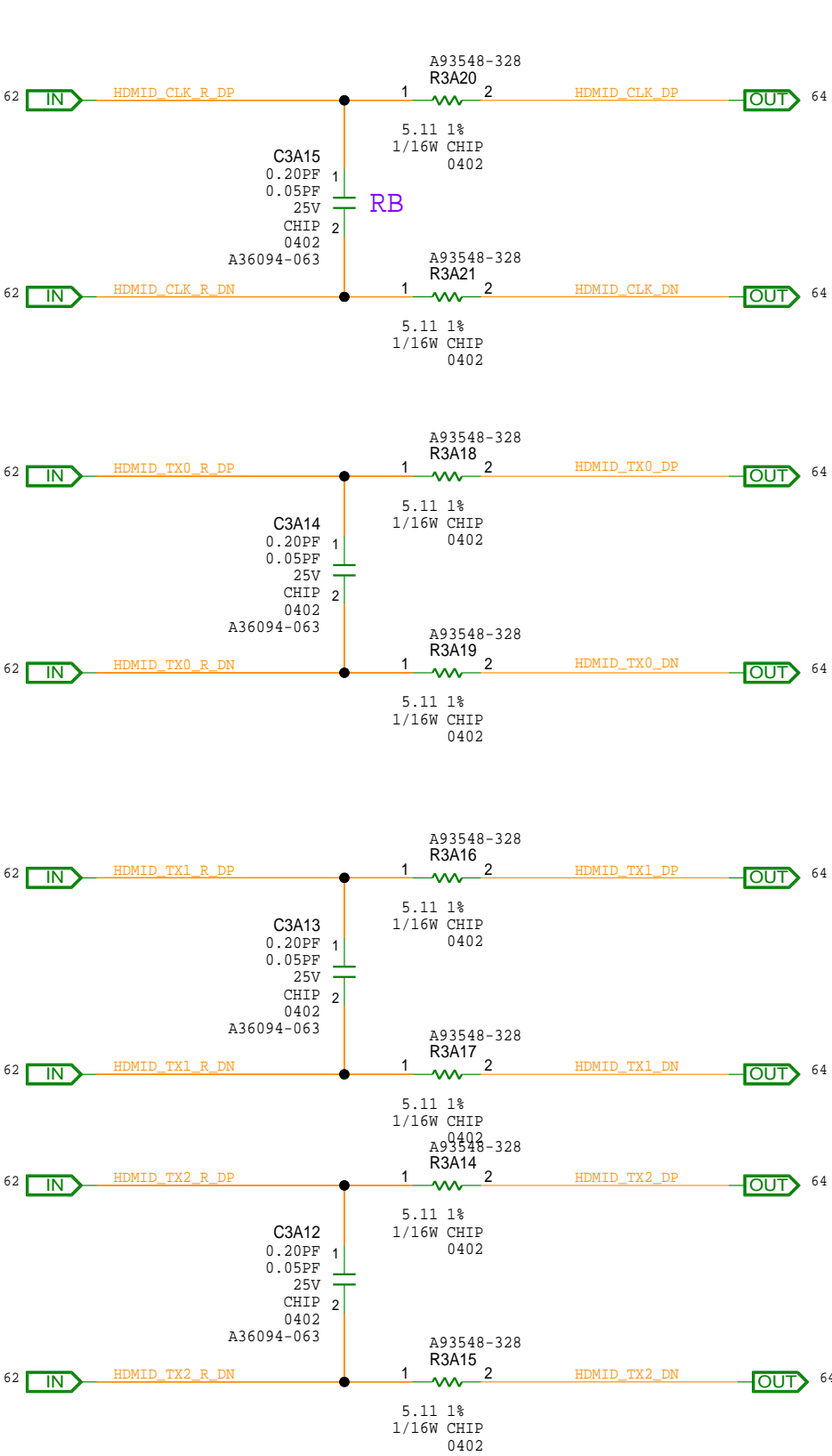
CAD NOTE:

COMMENT\_BODY

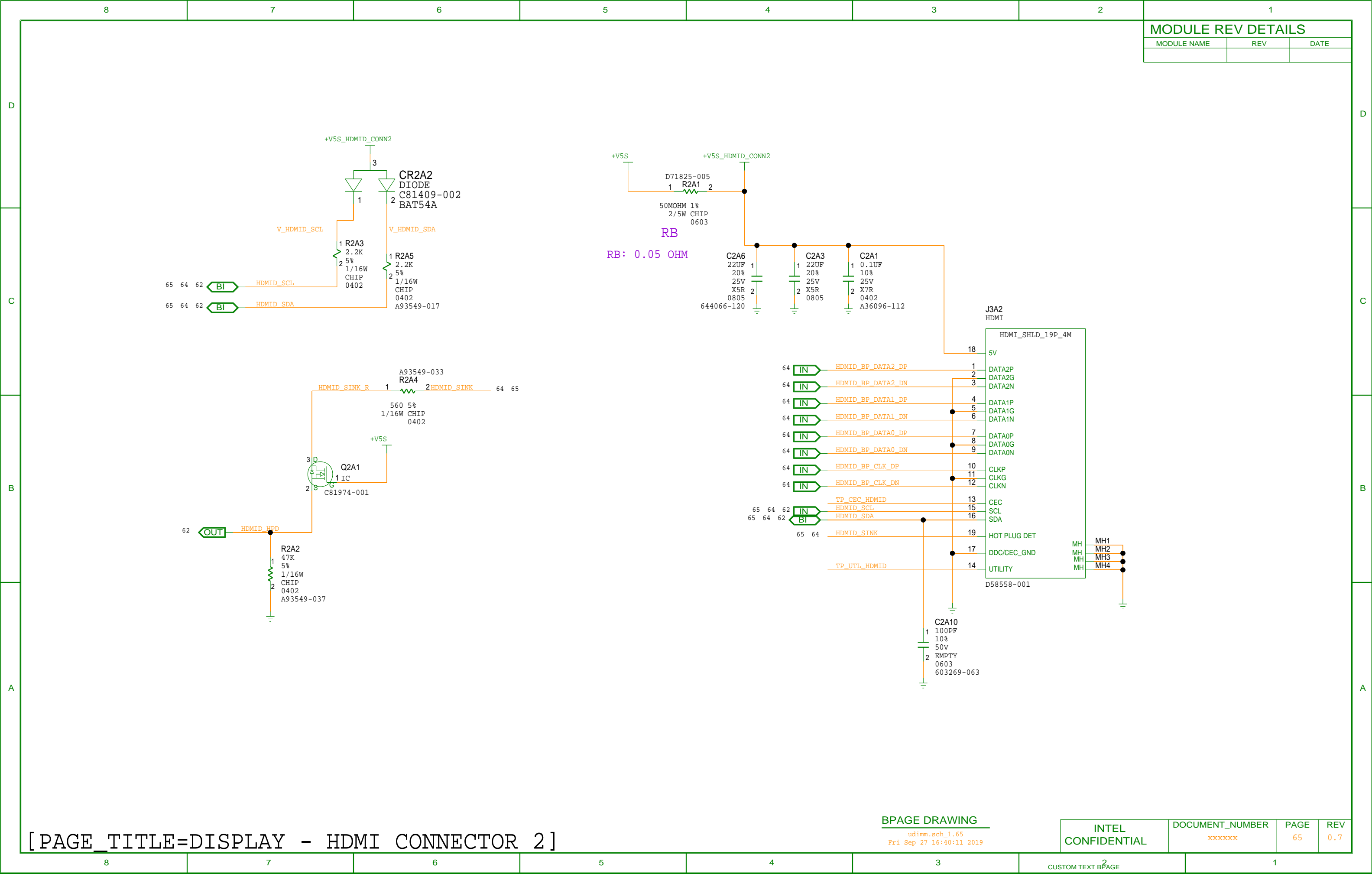
LSPCON RESET

MODULE REV DETAILS

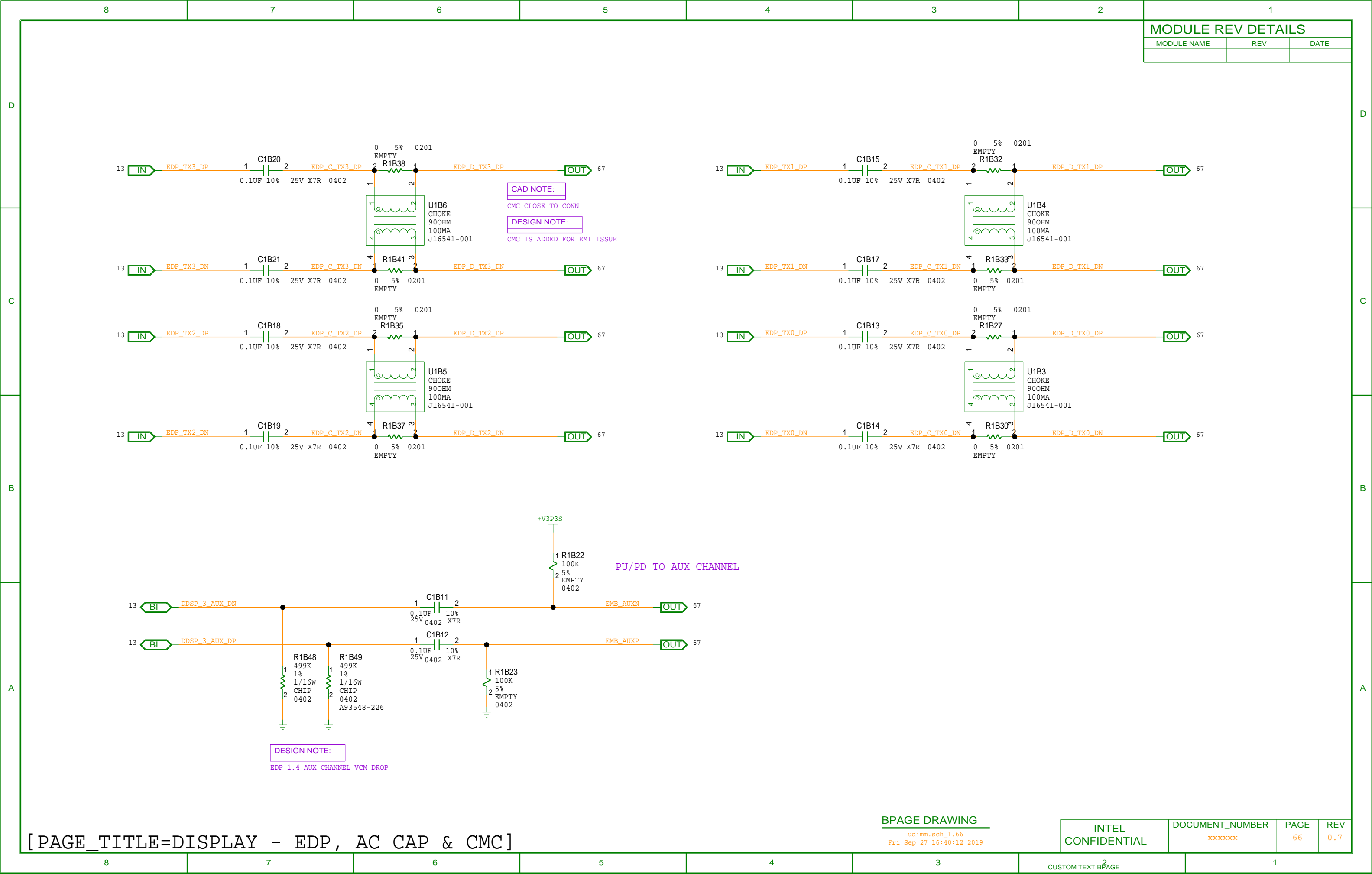
MODULE NAME	REV	DATE

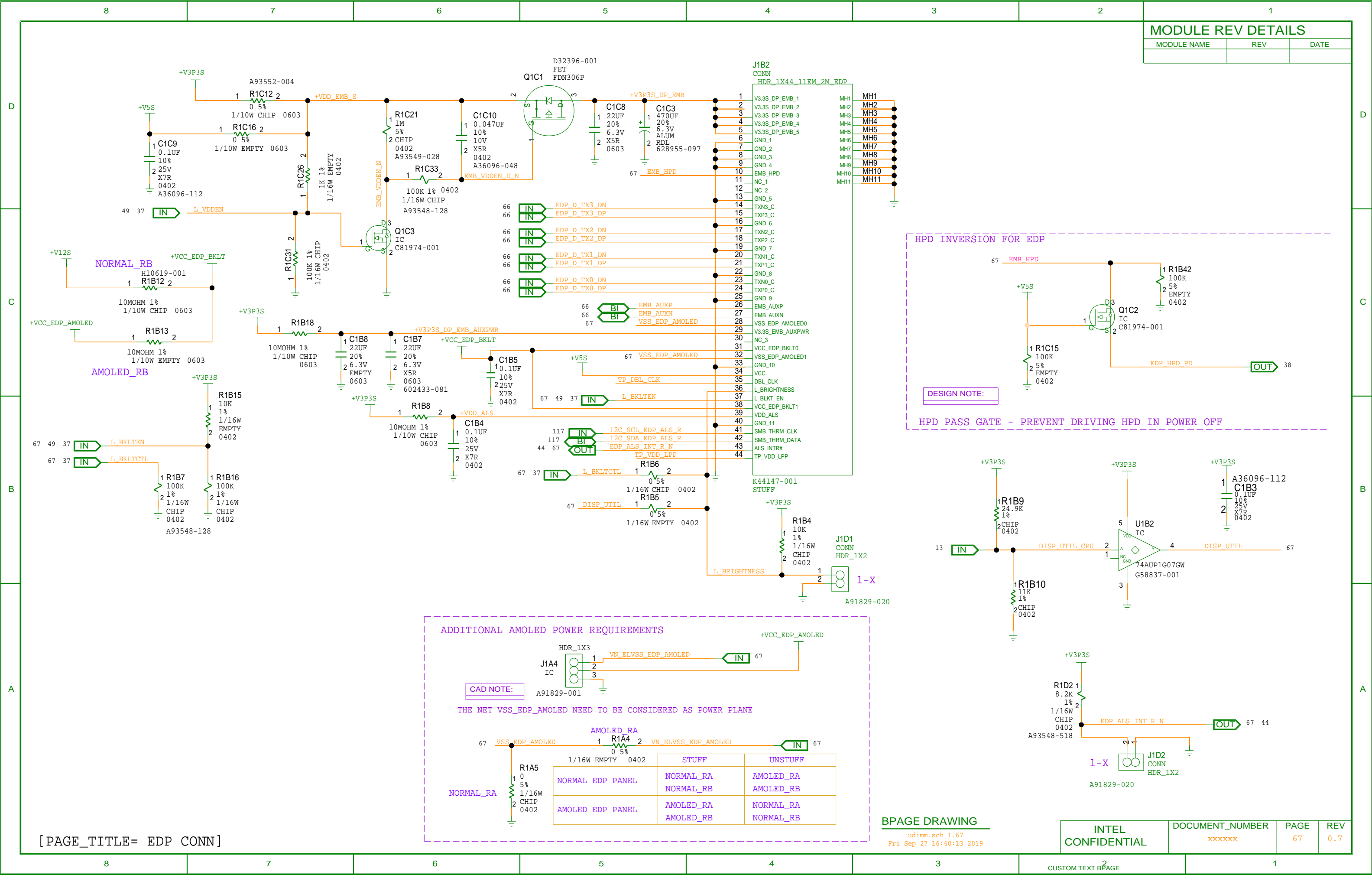


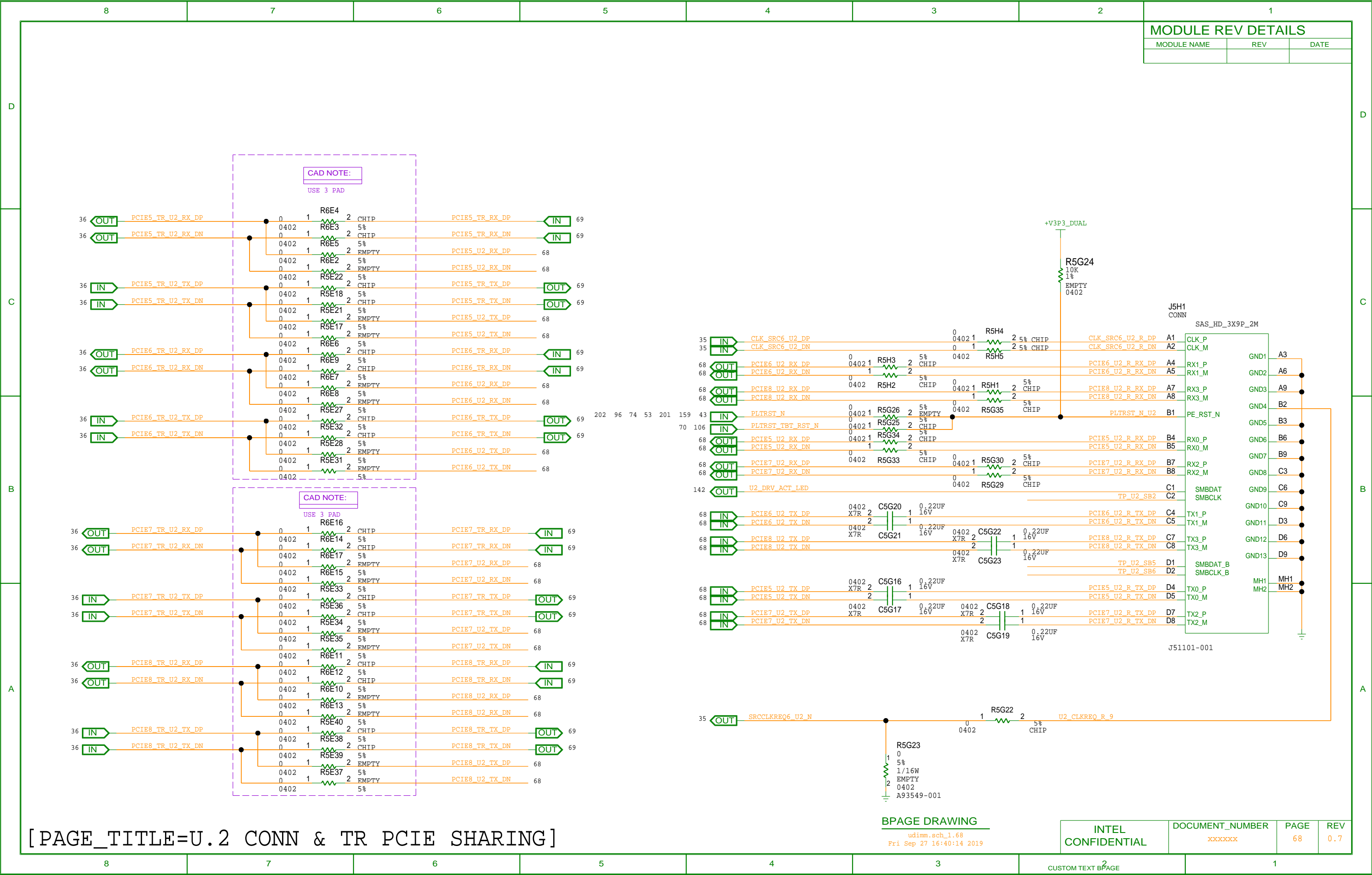


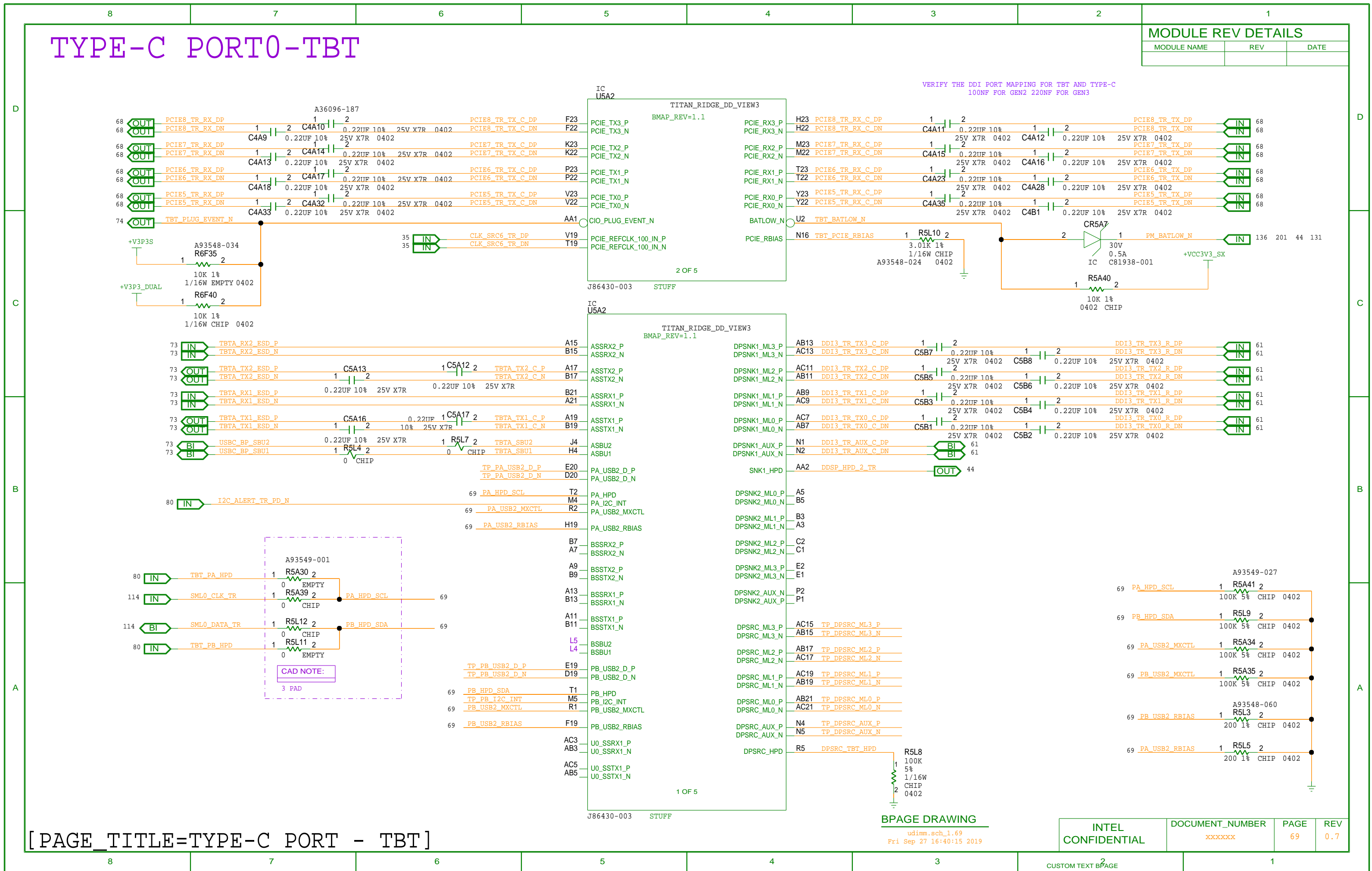


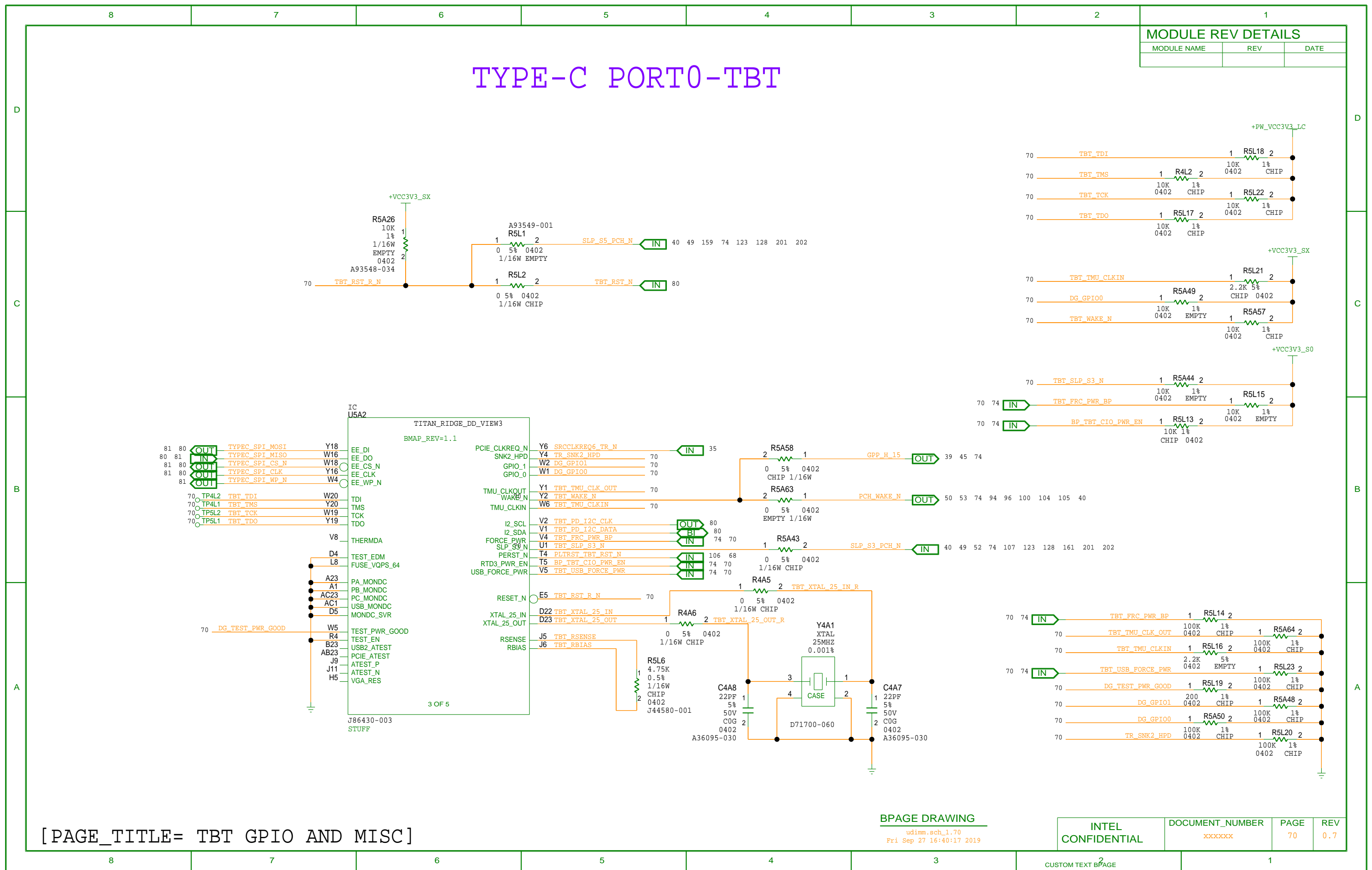








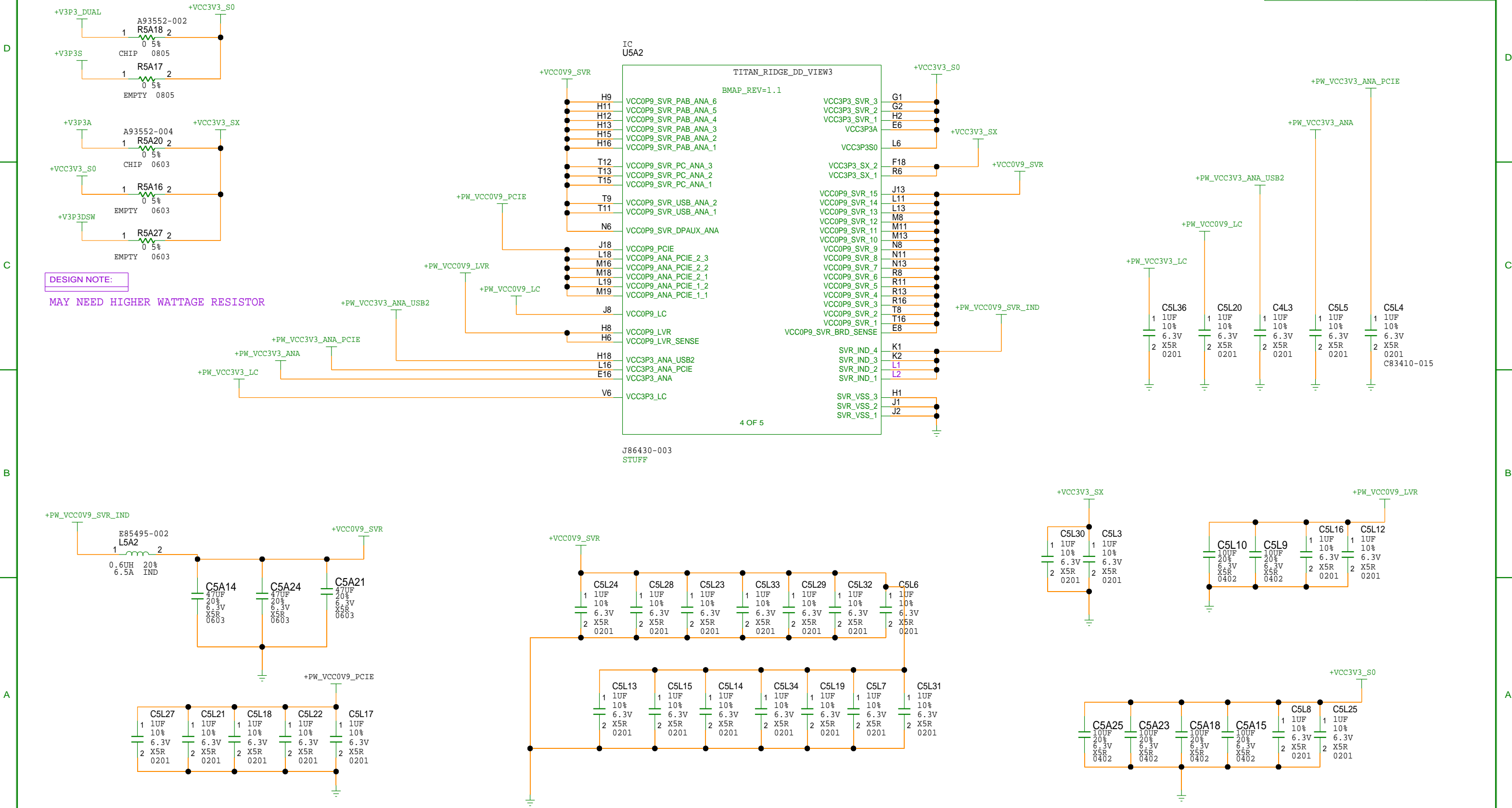




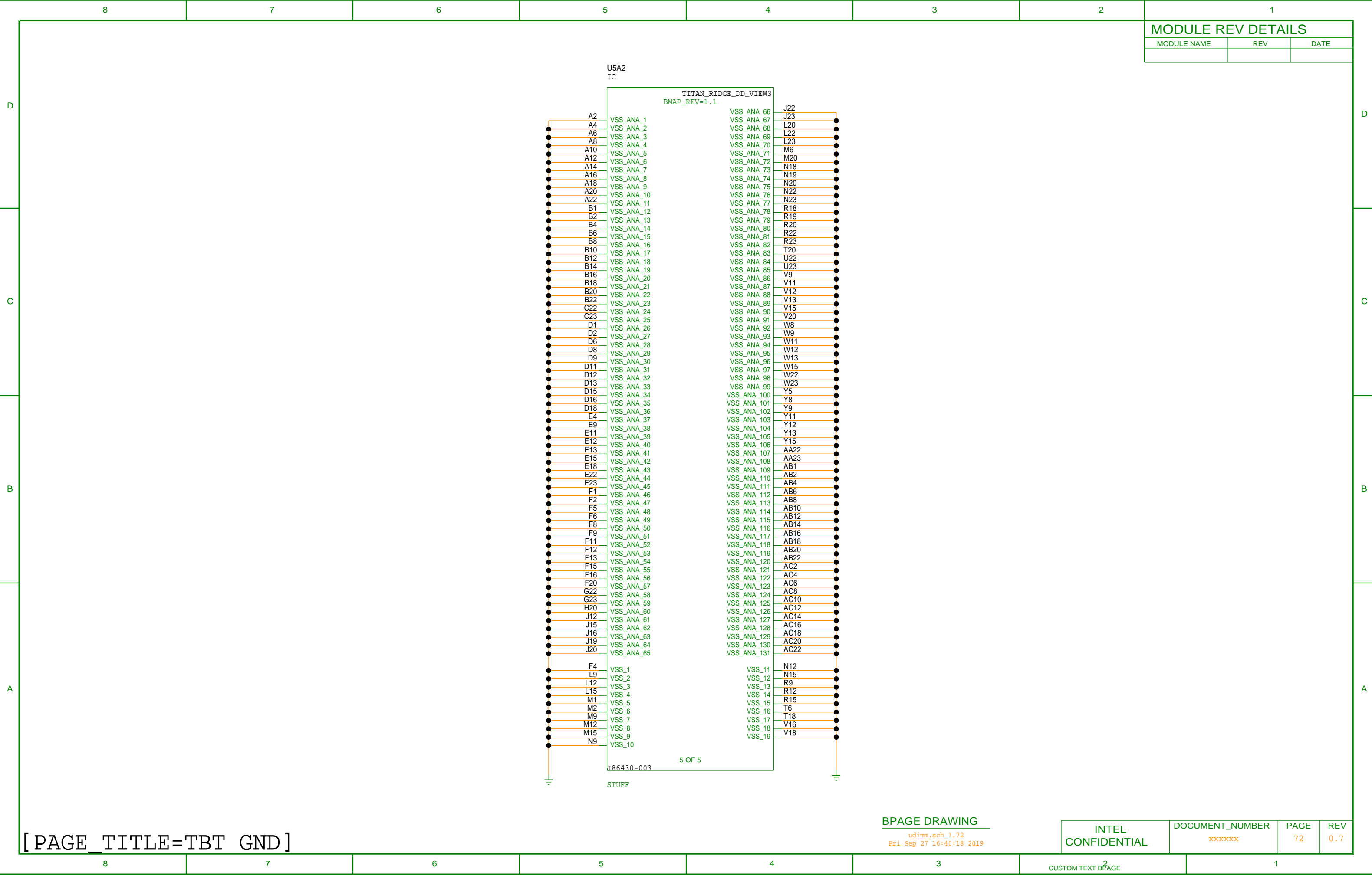
TYPE-C PORT0-TBT

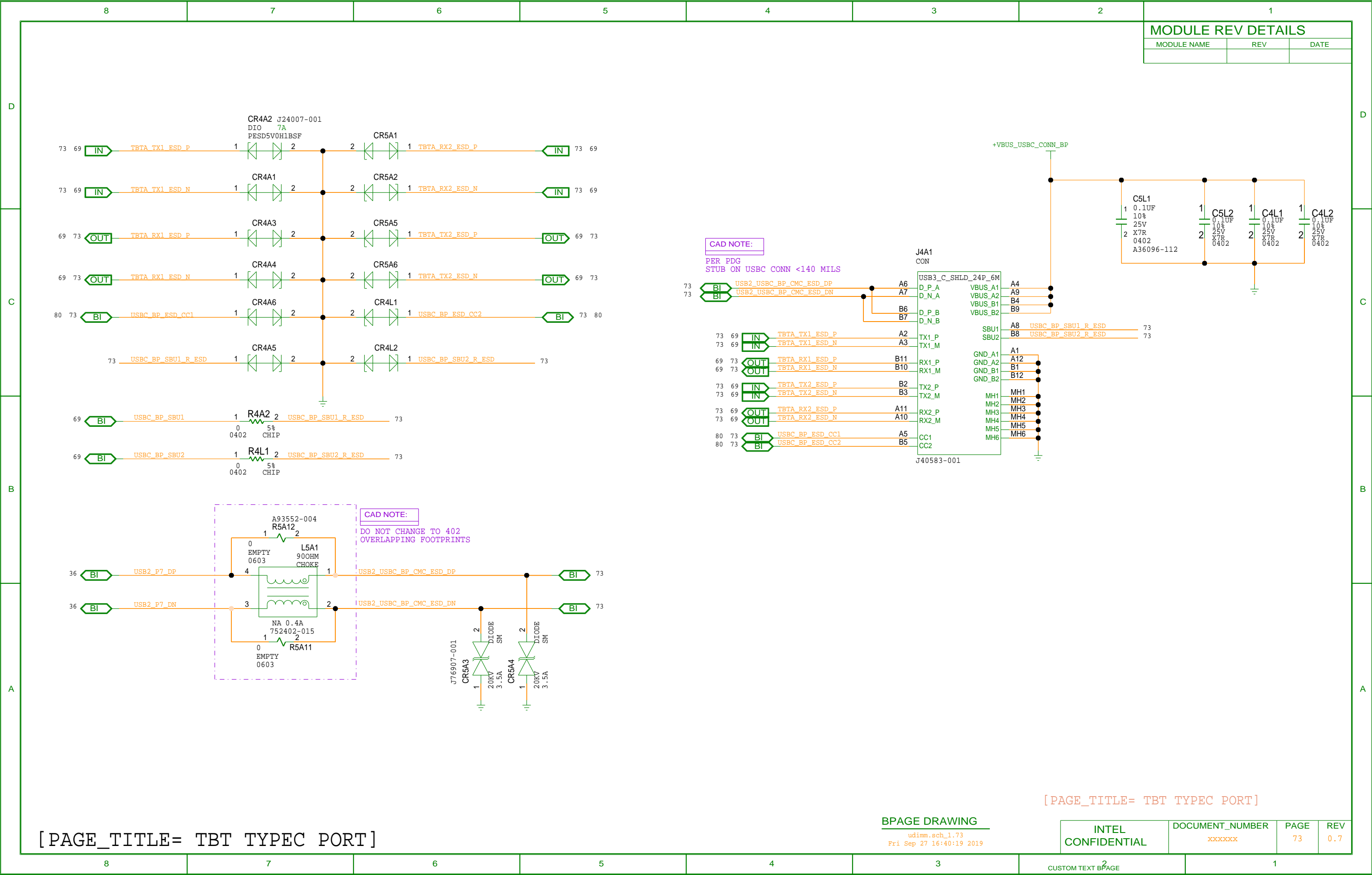
MODULE REV DETAILS

MODULE NAME	REV	DATE



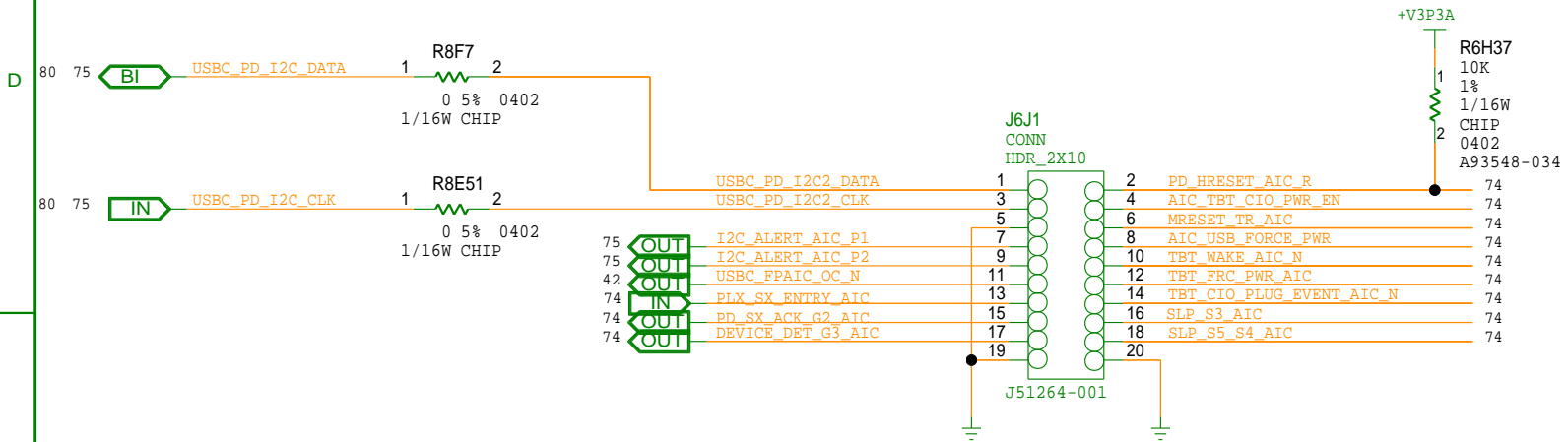




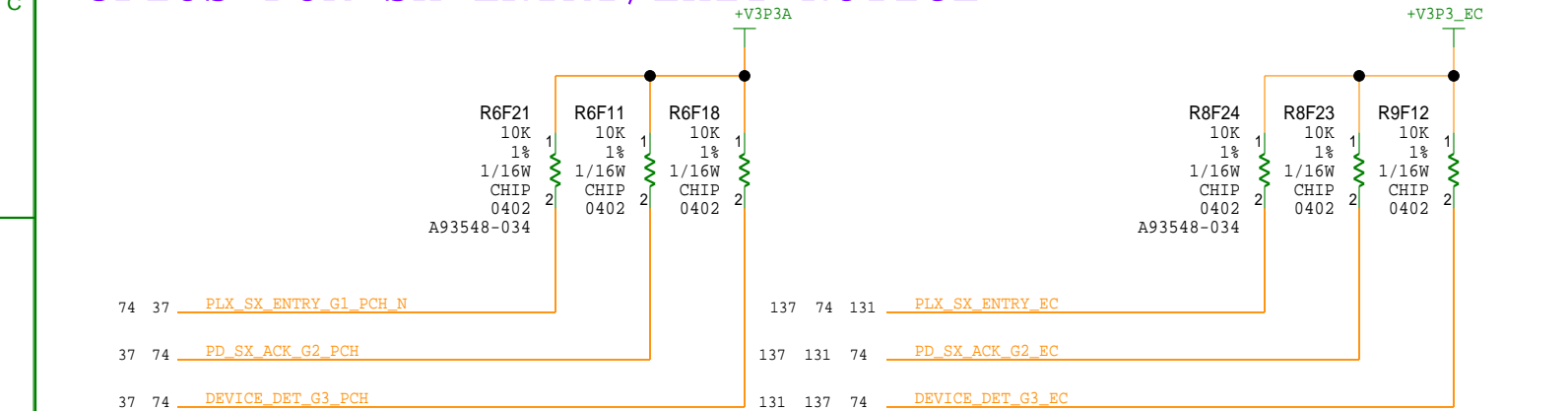




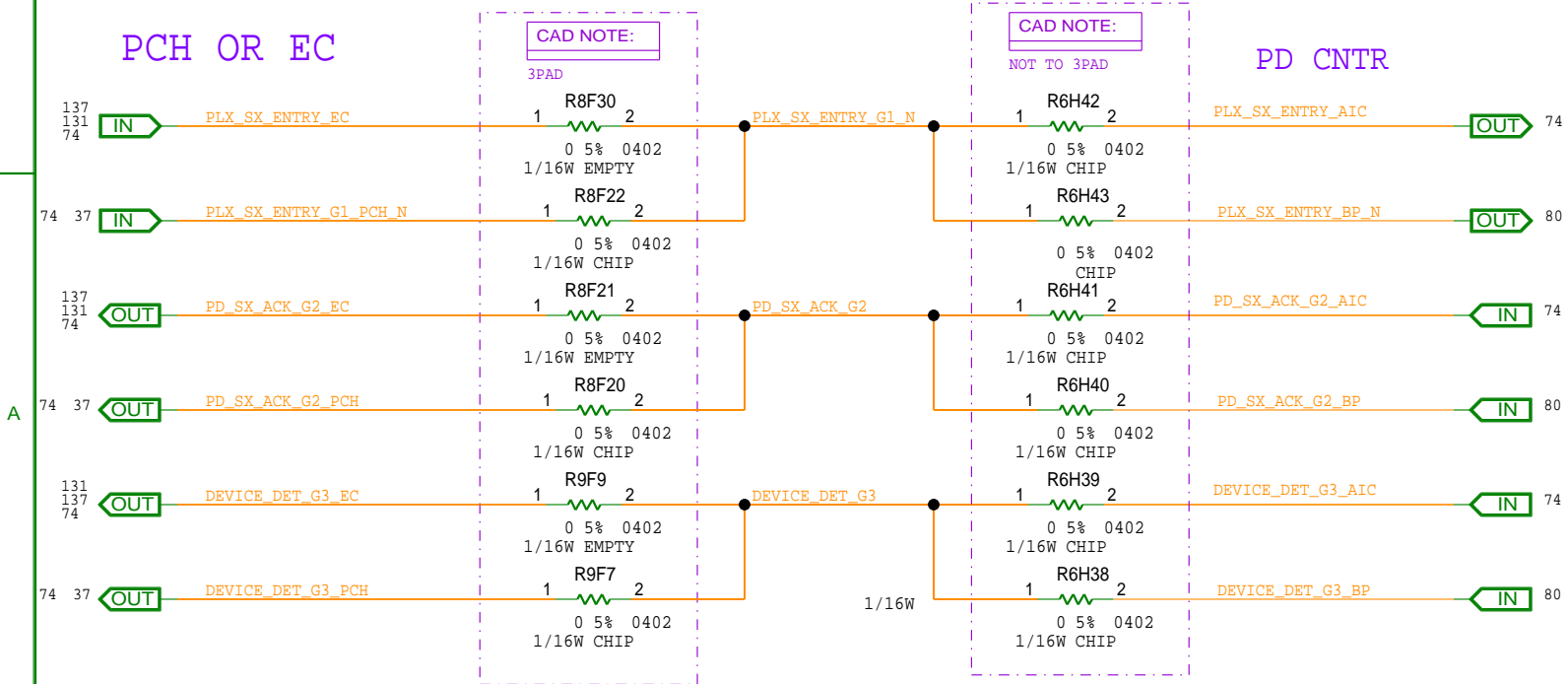
FP TYPE-C AIC SIDEBAND HEADER



GPIOS FOR SX ENTRY/EXIT NOTICE

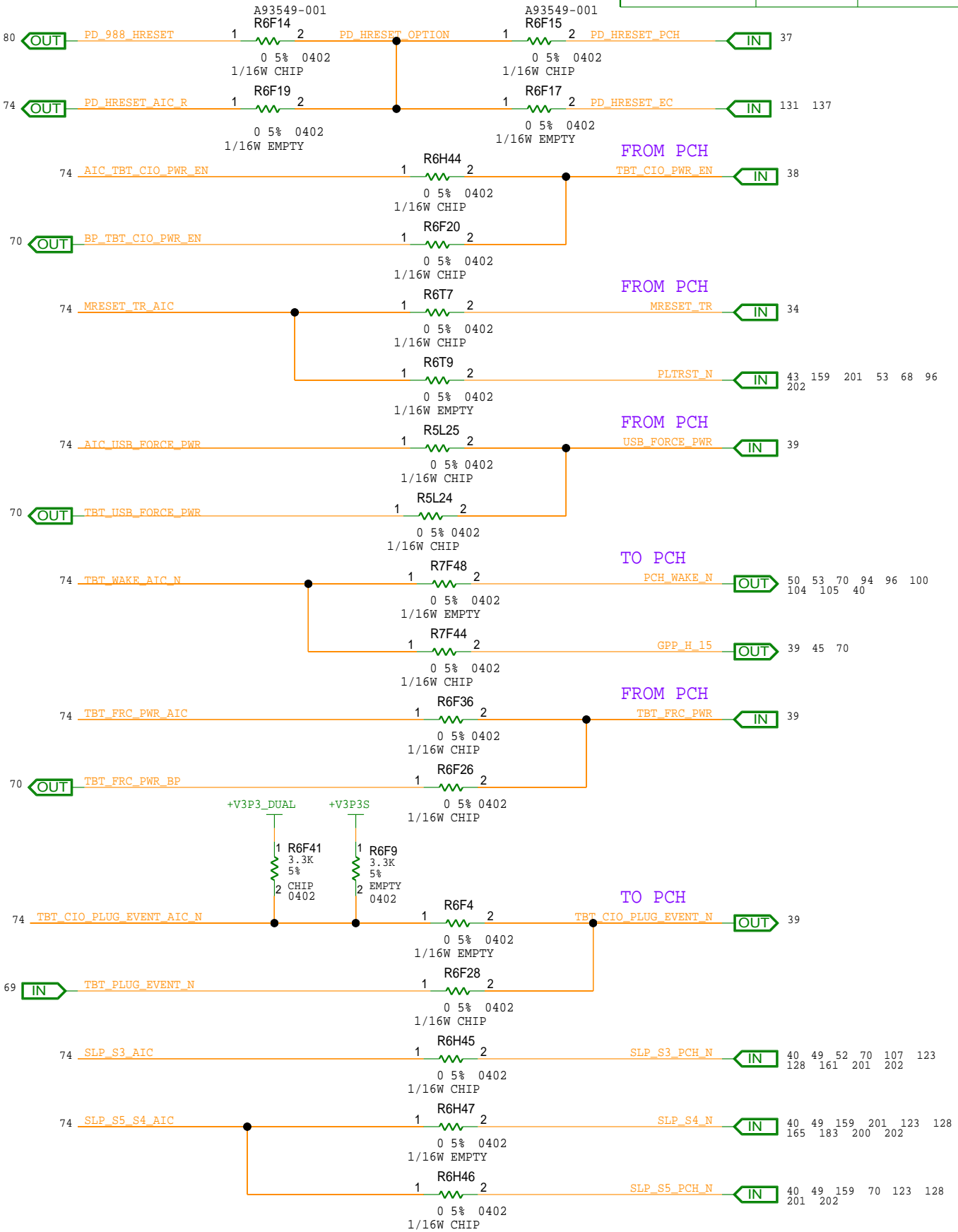


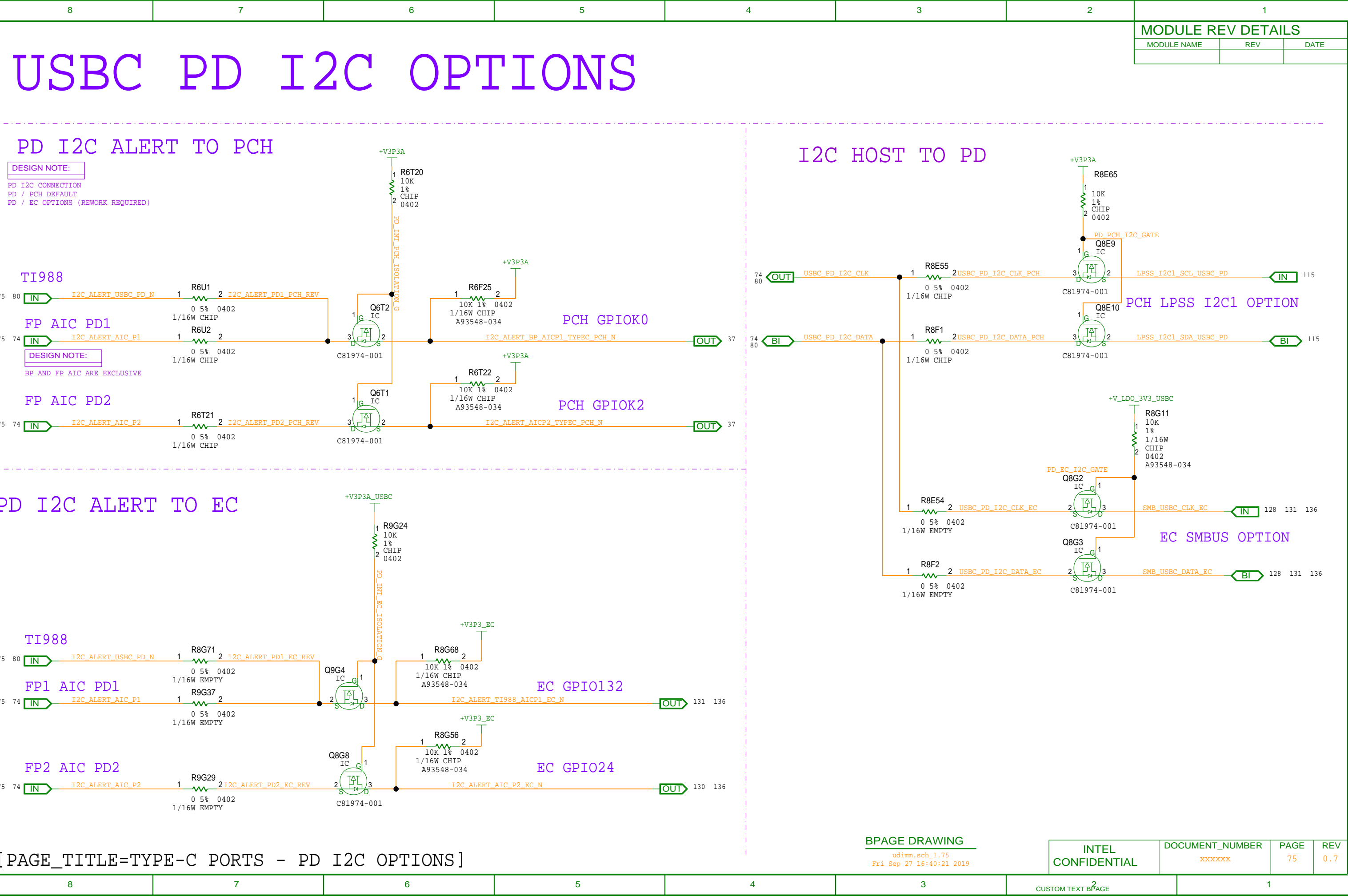
PCH OR EC



MODULE REV DETAILS

MODULE NAME	REV	DATE





MODULE NAME	REV	DATE

D



B



3 PAD

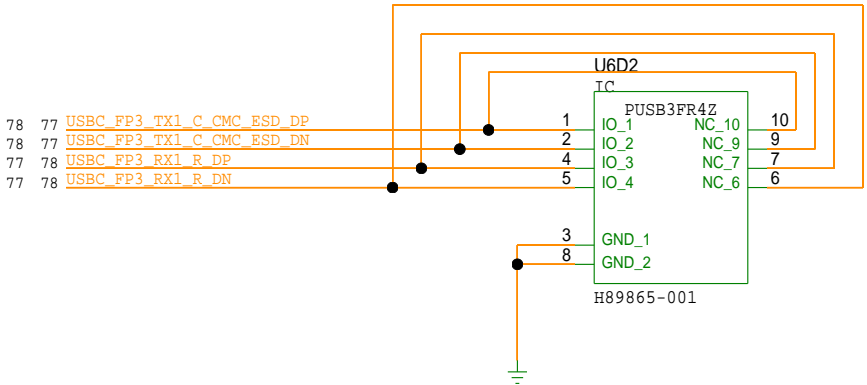
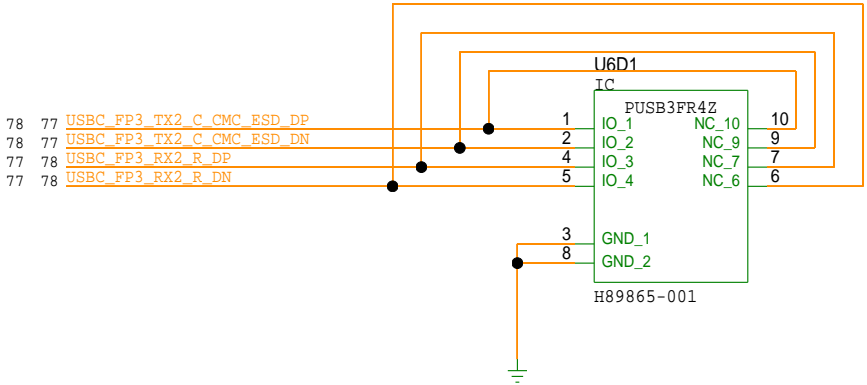
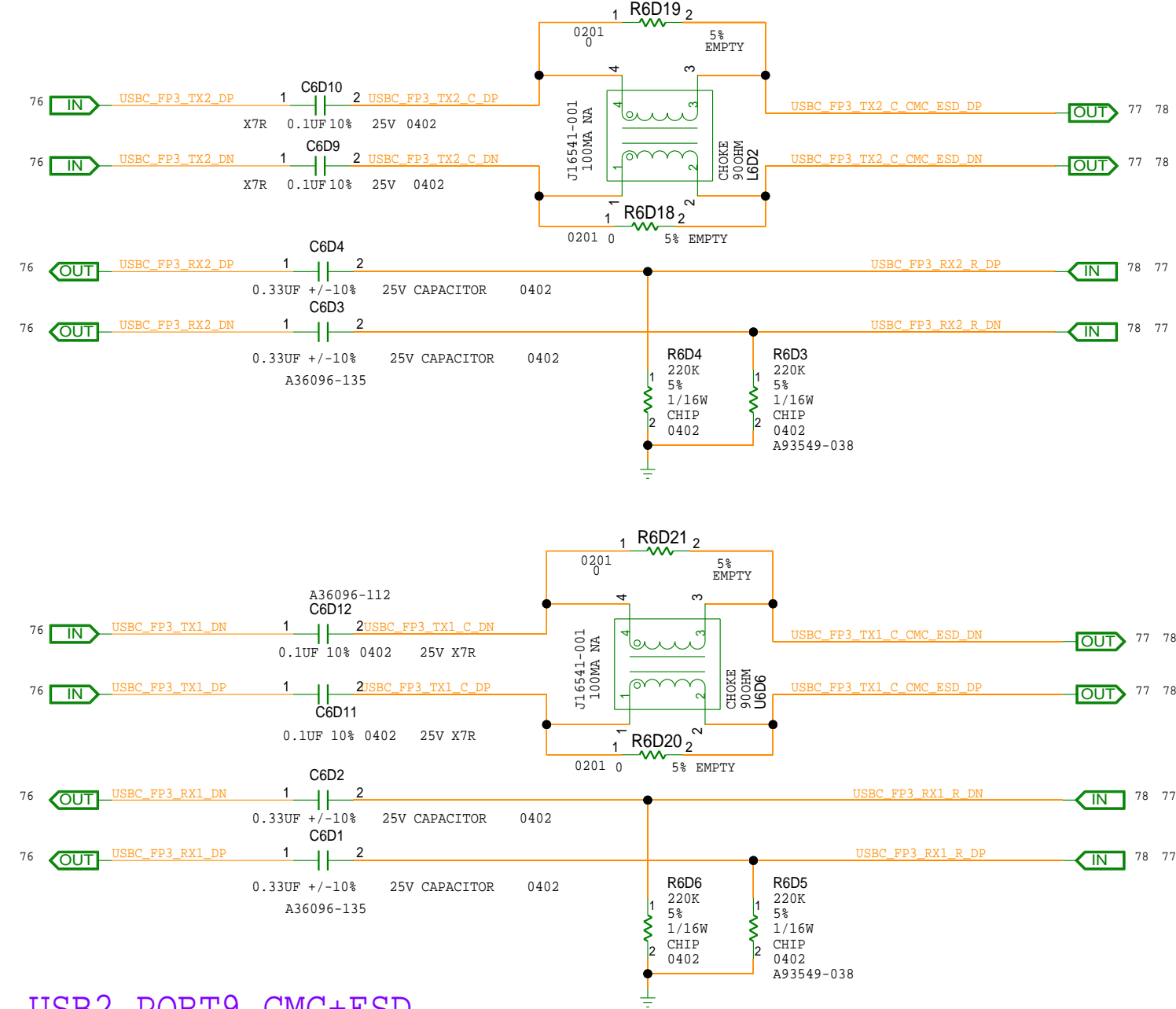


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Fri Sep 27 16:40:22 2019
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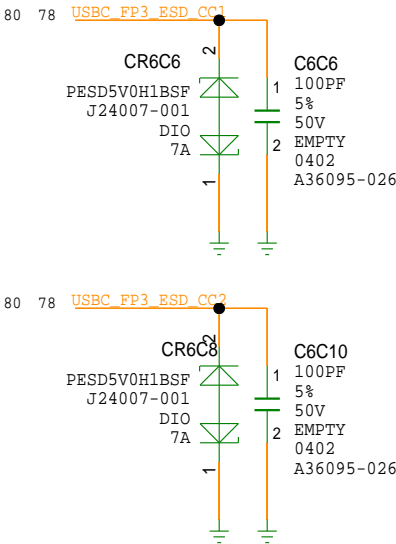
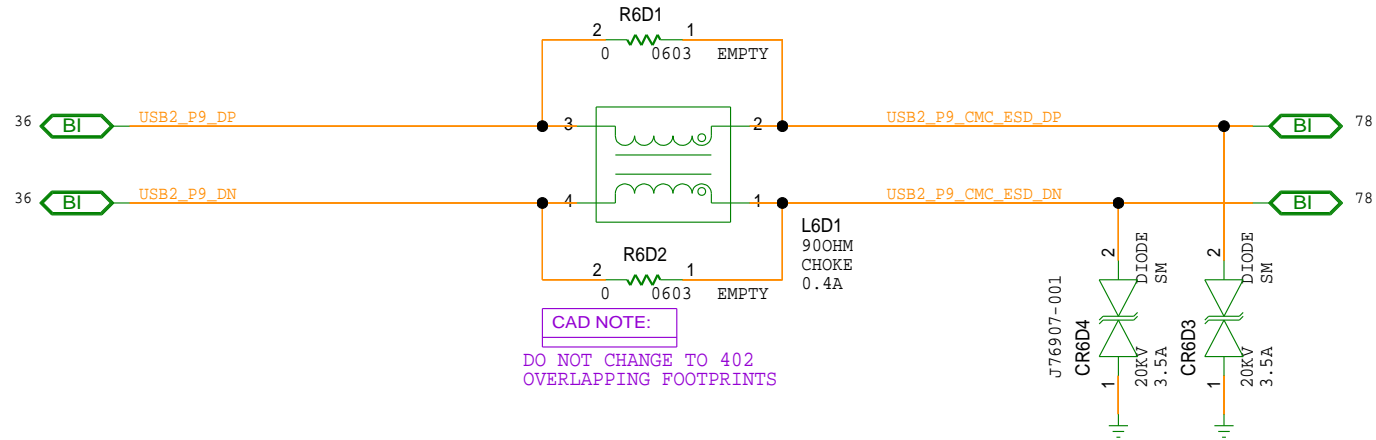
USB31 P6 WTIH 1:2 MUX CMC+ESD

MODULE REV DETAILS

MODULE NAME	REV	DATE

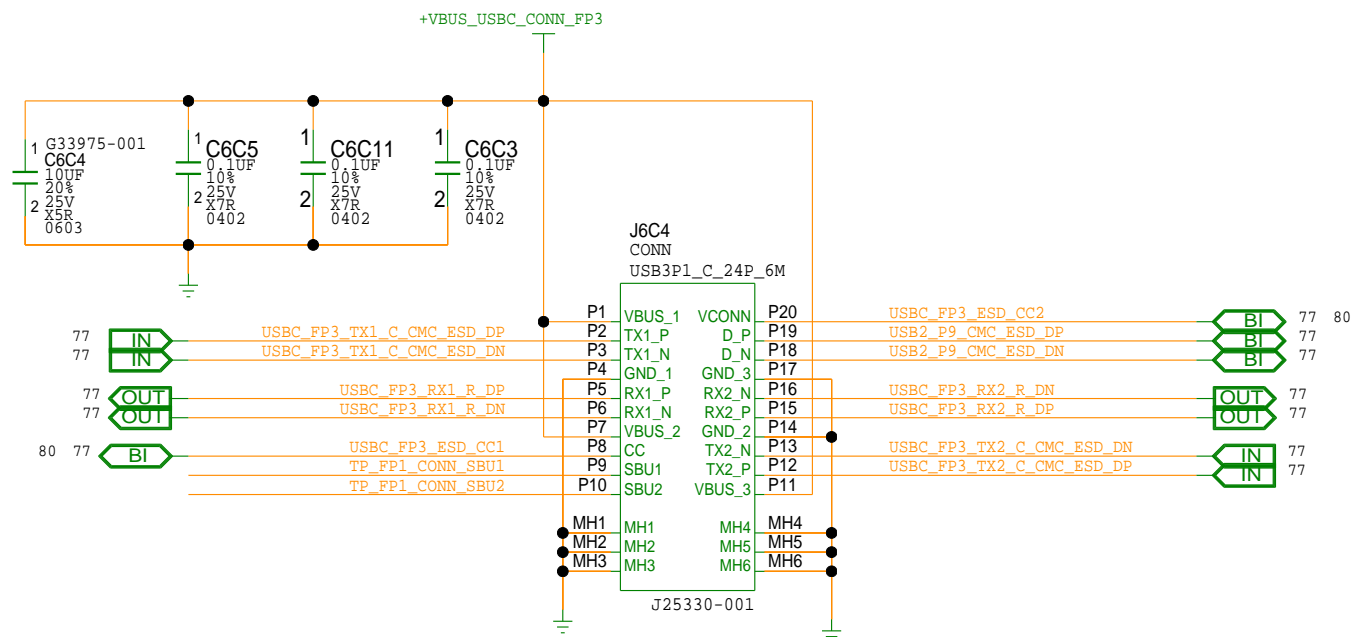


USB2 PORT9 CMC+ESD

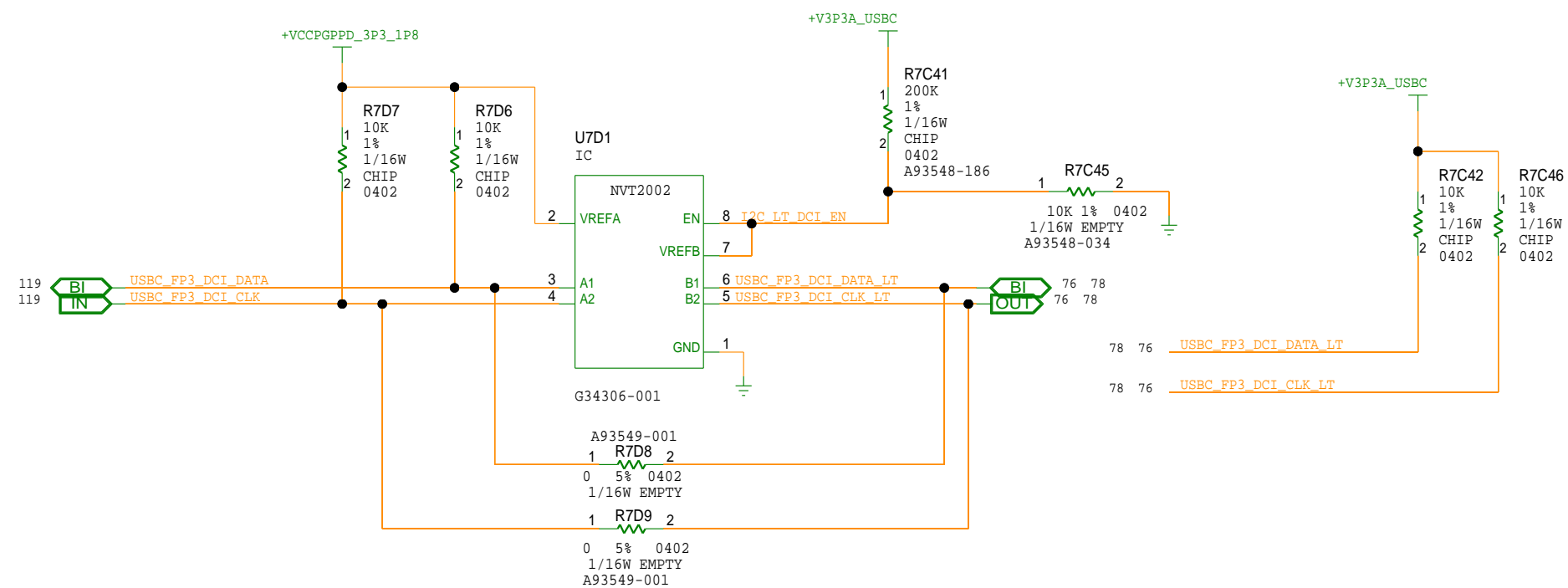




MODULE REV DETAILS		
MODULE NAME	REV	DATE



## LEVEL SHIFTER FOR DCI OF FP TYPE-C PORT



[PAGE\_TITLE- TYPE-C FP PORT - HEADER]

BPAGE DRAWING

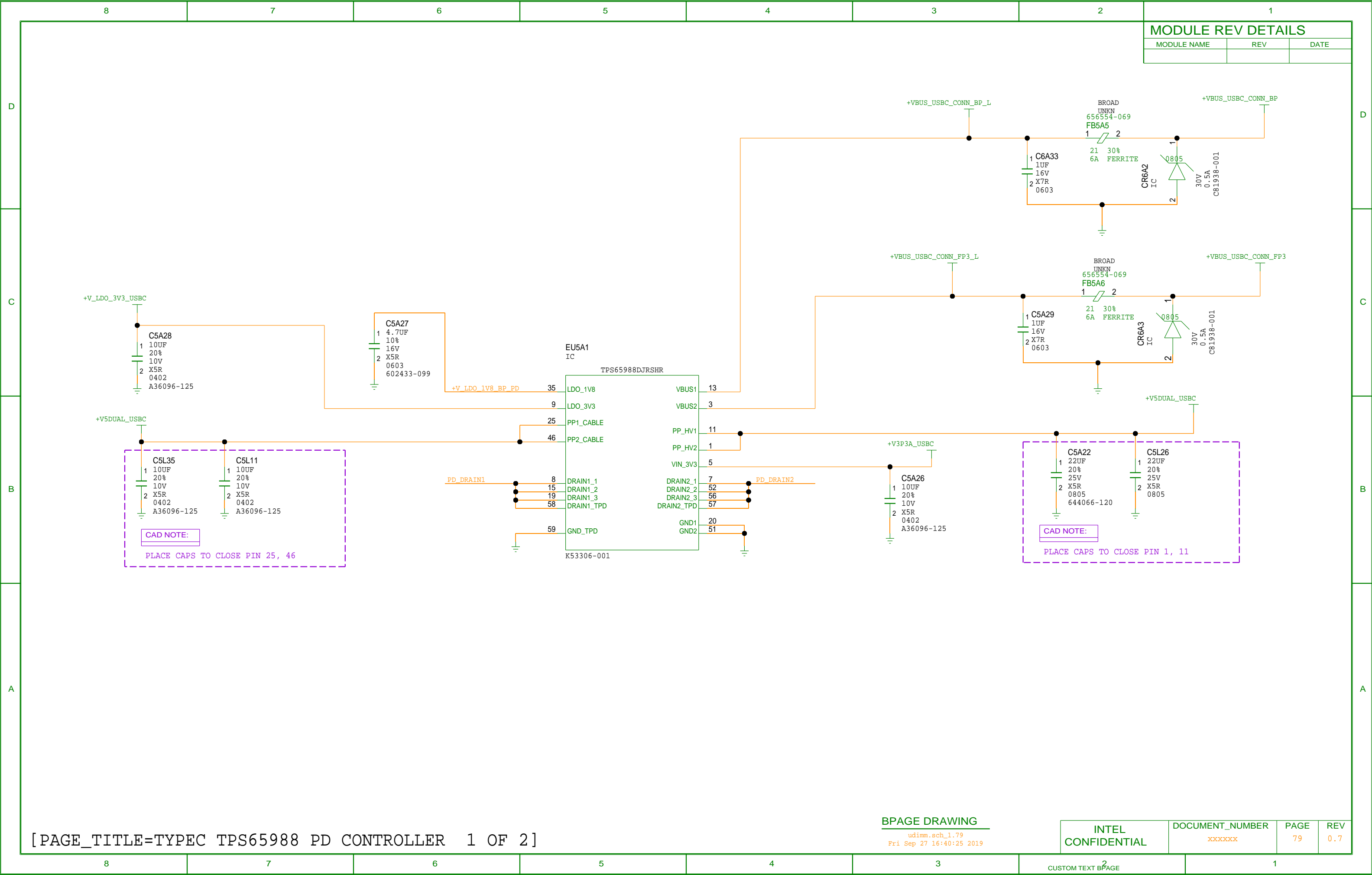
udimm.sch\_1.78  
Fri Sep 27 16:40:24 2019

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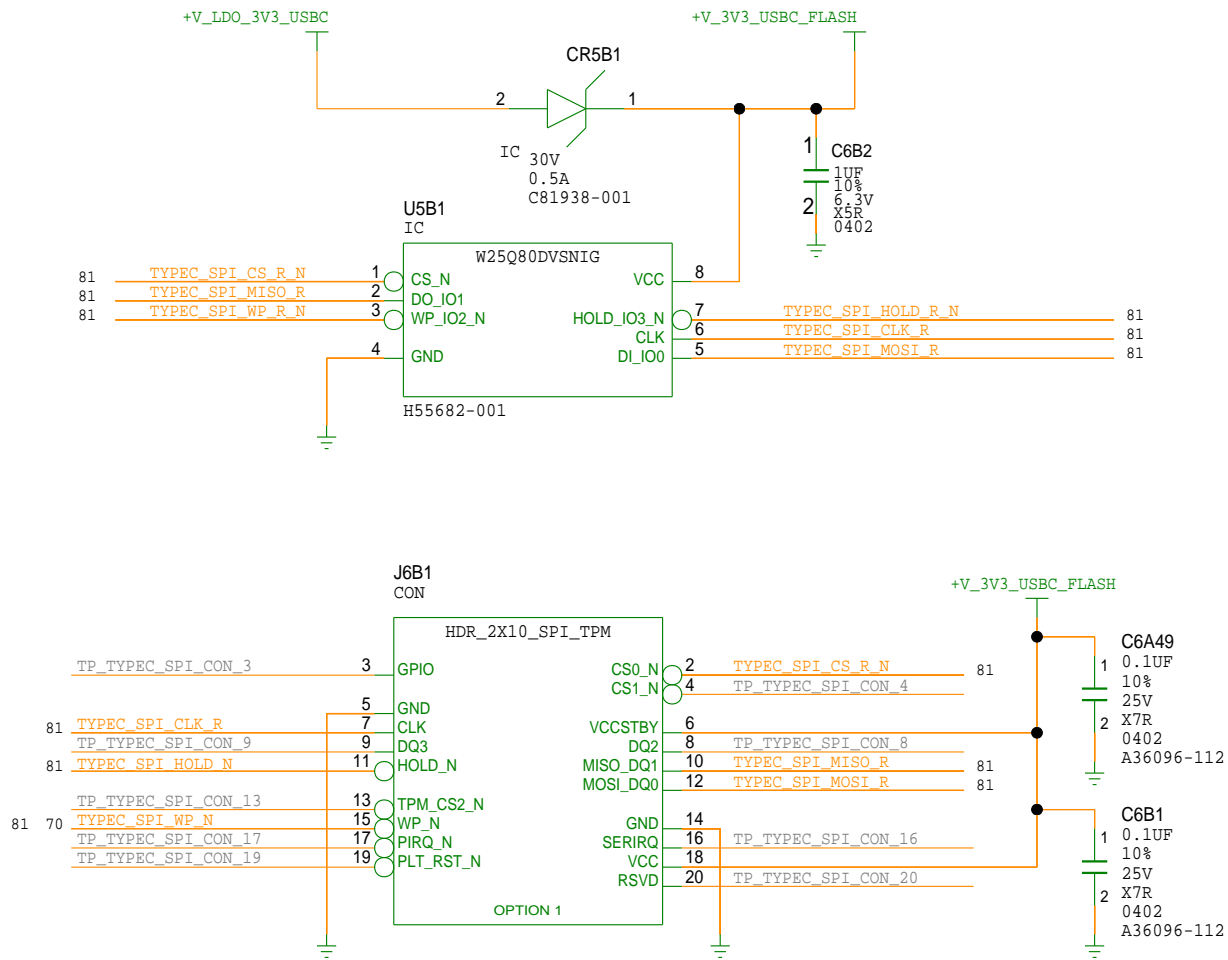
REV







INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxx	PAGE 81	REV 0.7
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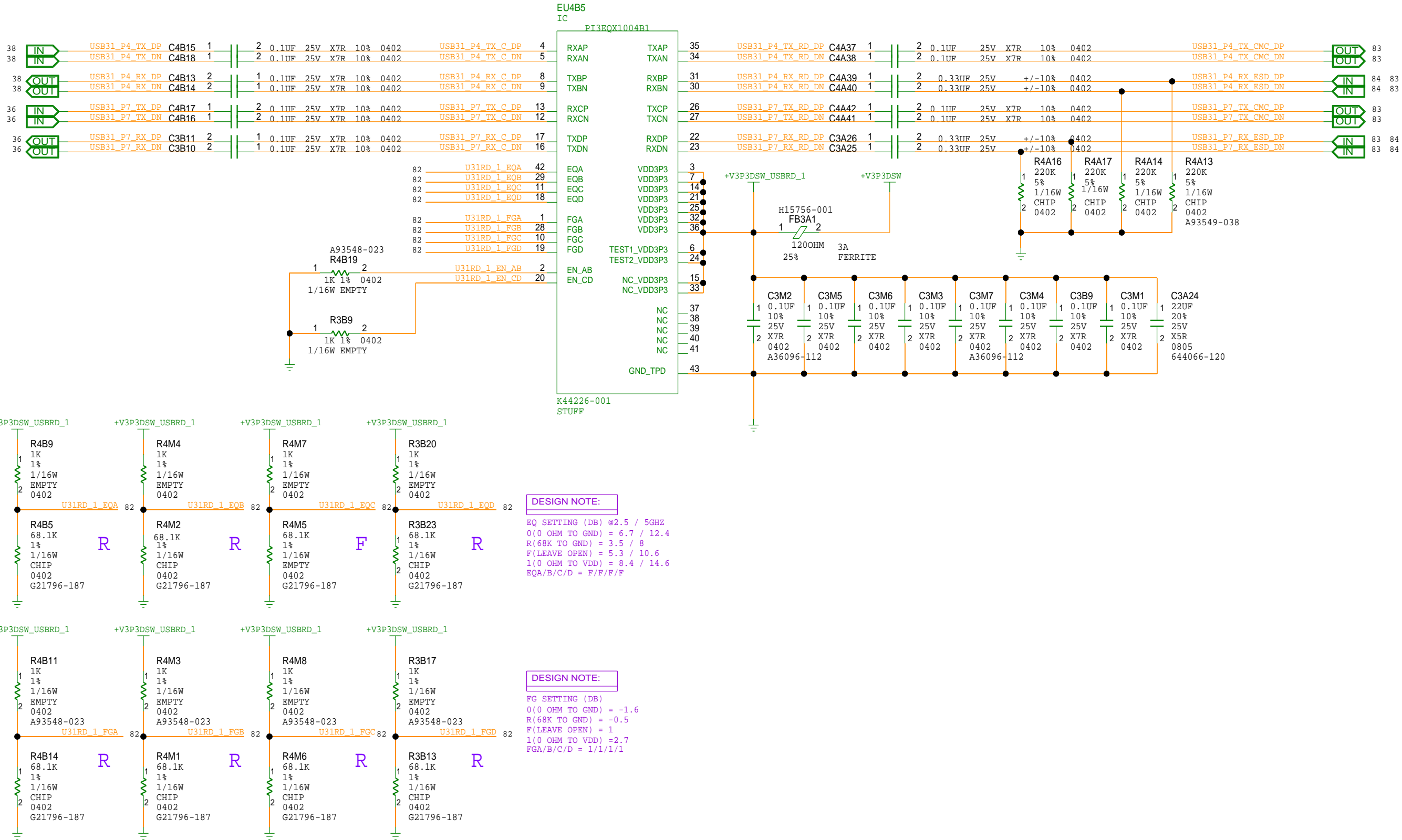




USB3.1 TYPE-A BACK PANEL - REDRIVER  
PORT4/7

MODULE REV DETAILS

MODULE NAME	REV	DATE



BPAGE DRAWING

udimm.sch\_1.82  
Fri Sep 27 16:40:27 2019

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CONFIDENTIAL

DOCUMENT\_NUMBER

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82

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0.7

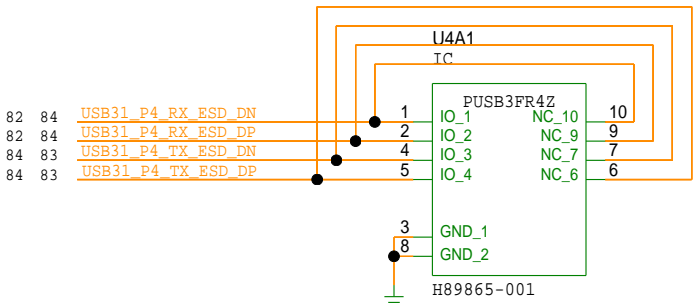
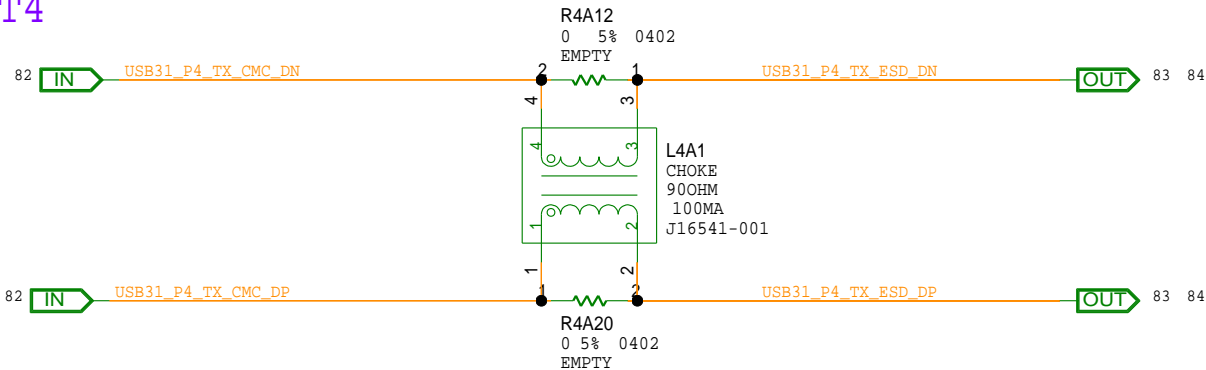
[PAGE\_TITLE=USB3.1 TYPE-A BACK PANEL #4#7 - REDRIVERS]

MODULE REV DETAILS

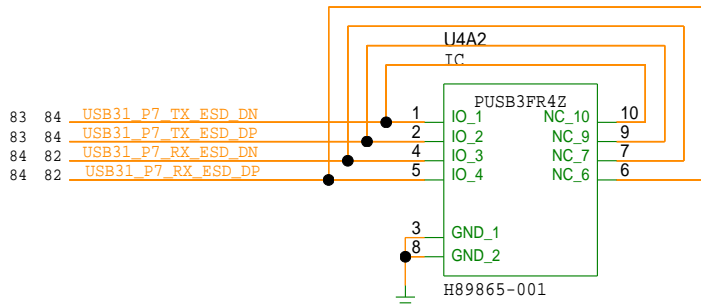
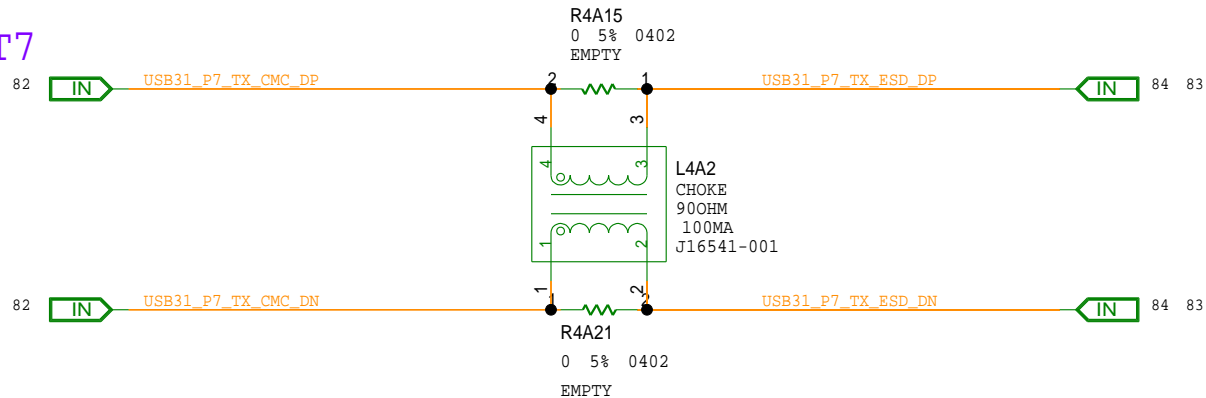
MODULE NAME	REV	DATE

USB3.1 TYPE-A BACK PANEL - CMC+ESD

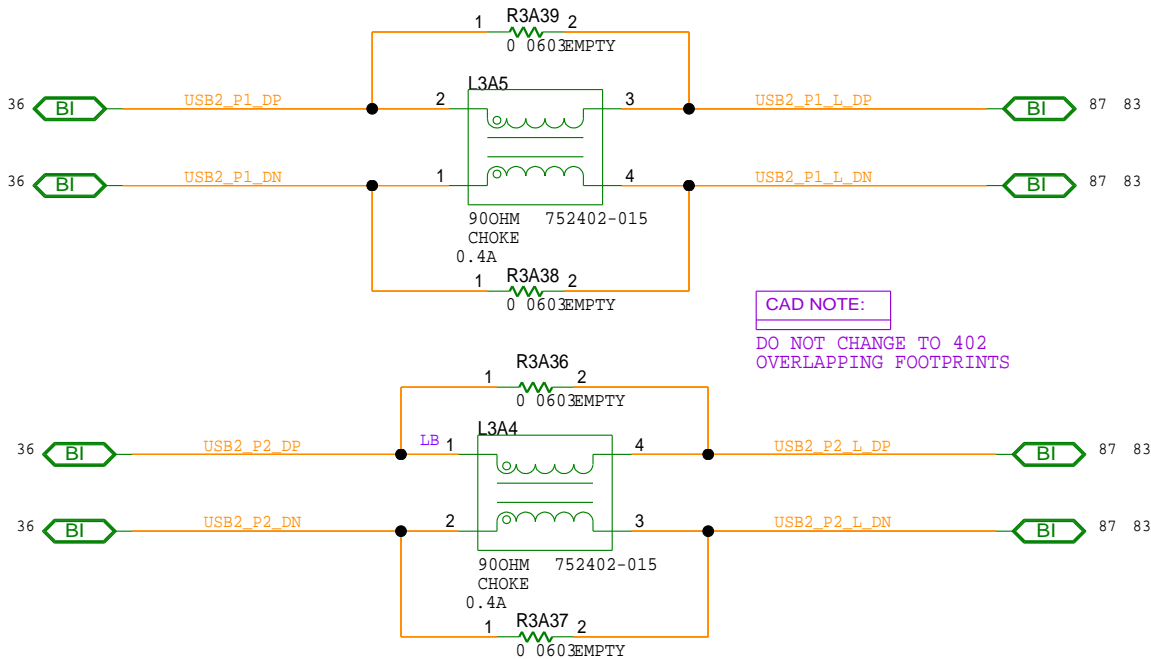
USB3.1 PORT4



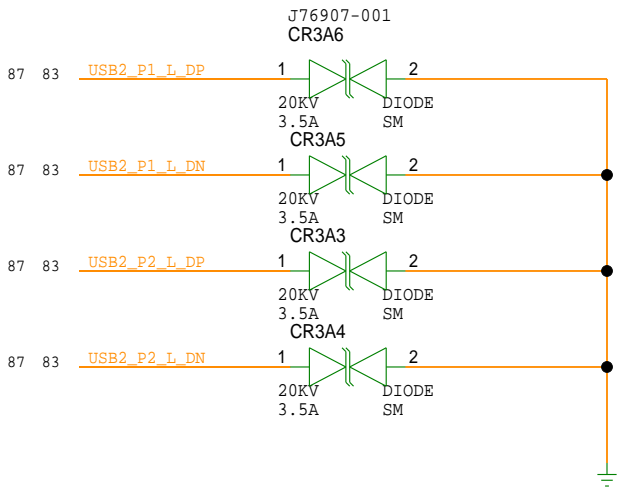
USB3.1 PORT7



USB2.0 PORT1/2 CMC+ESD



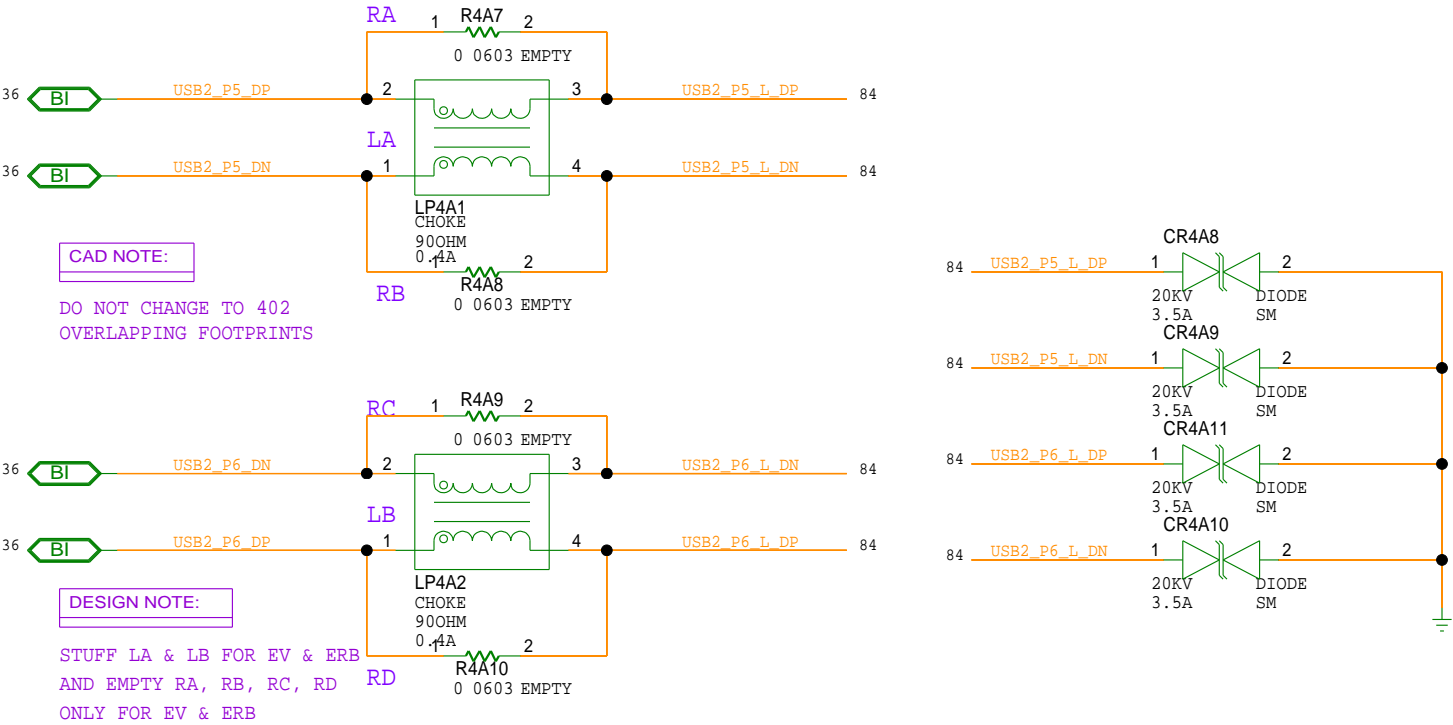
CAD NOTE:  
DO NOT CHANGE TO 402  
OVERLAPPING FOOTPRINTS



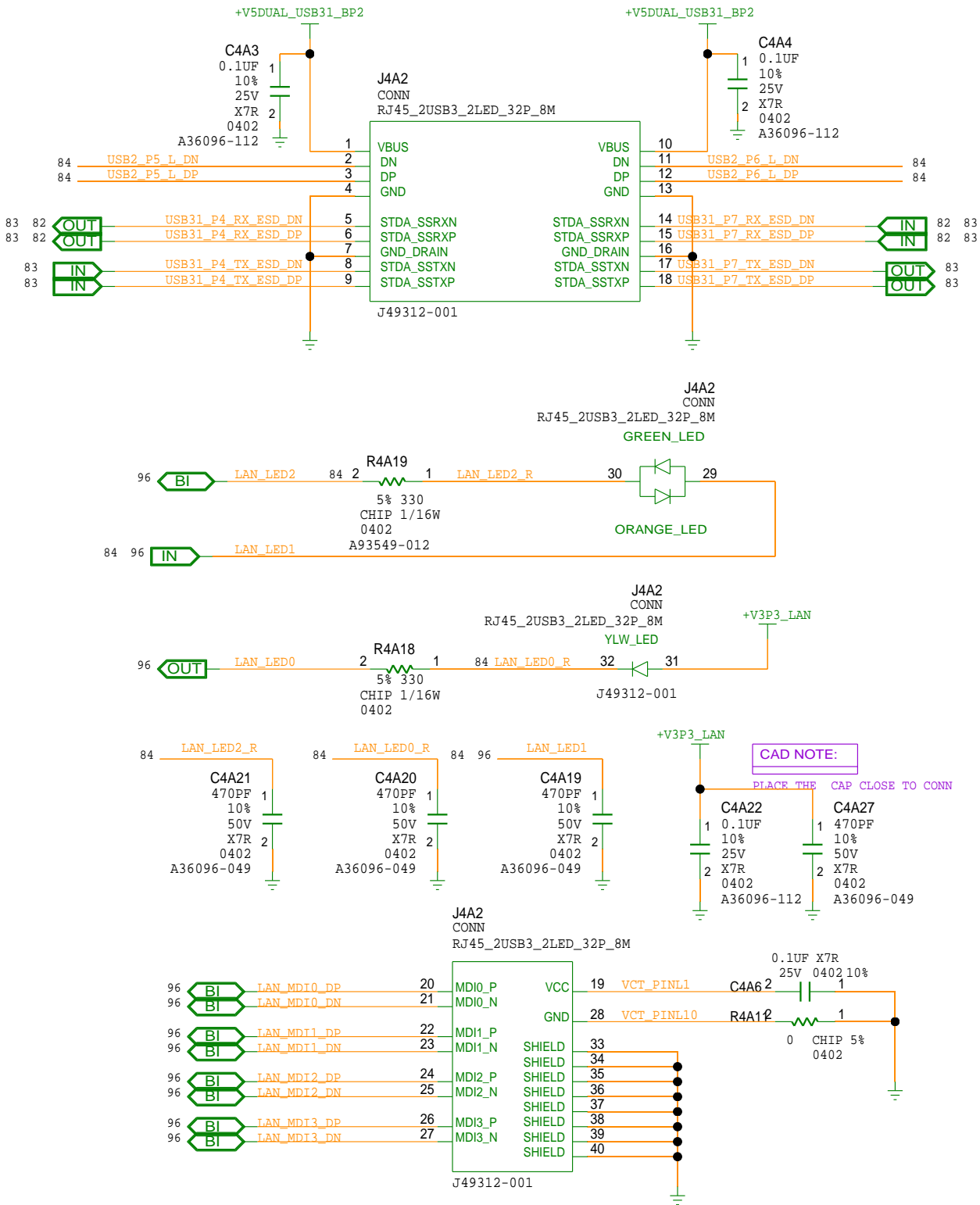
MODULE REV DETAILS

MODULE NAME	REV	DATE

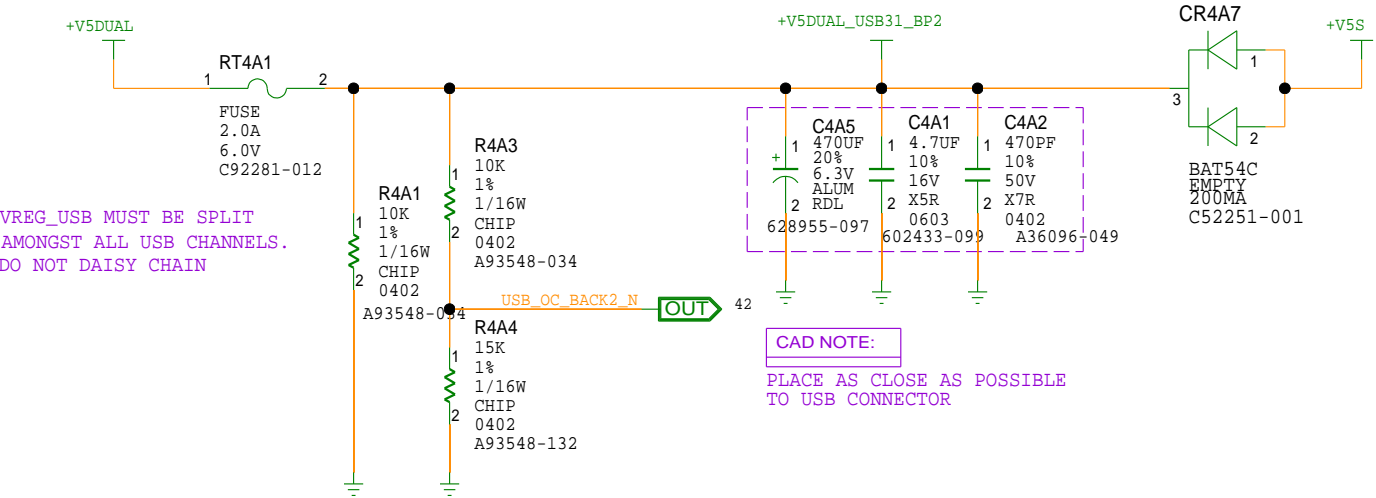
USB2.0 CMC+ESD



RJ45 & DUAL USB3.1 TYPEA STACK CONNECTOR



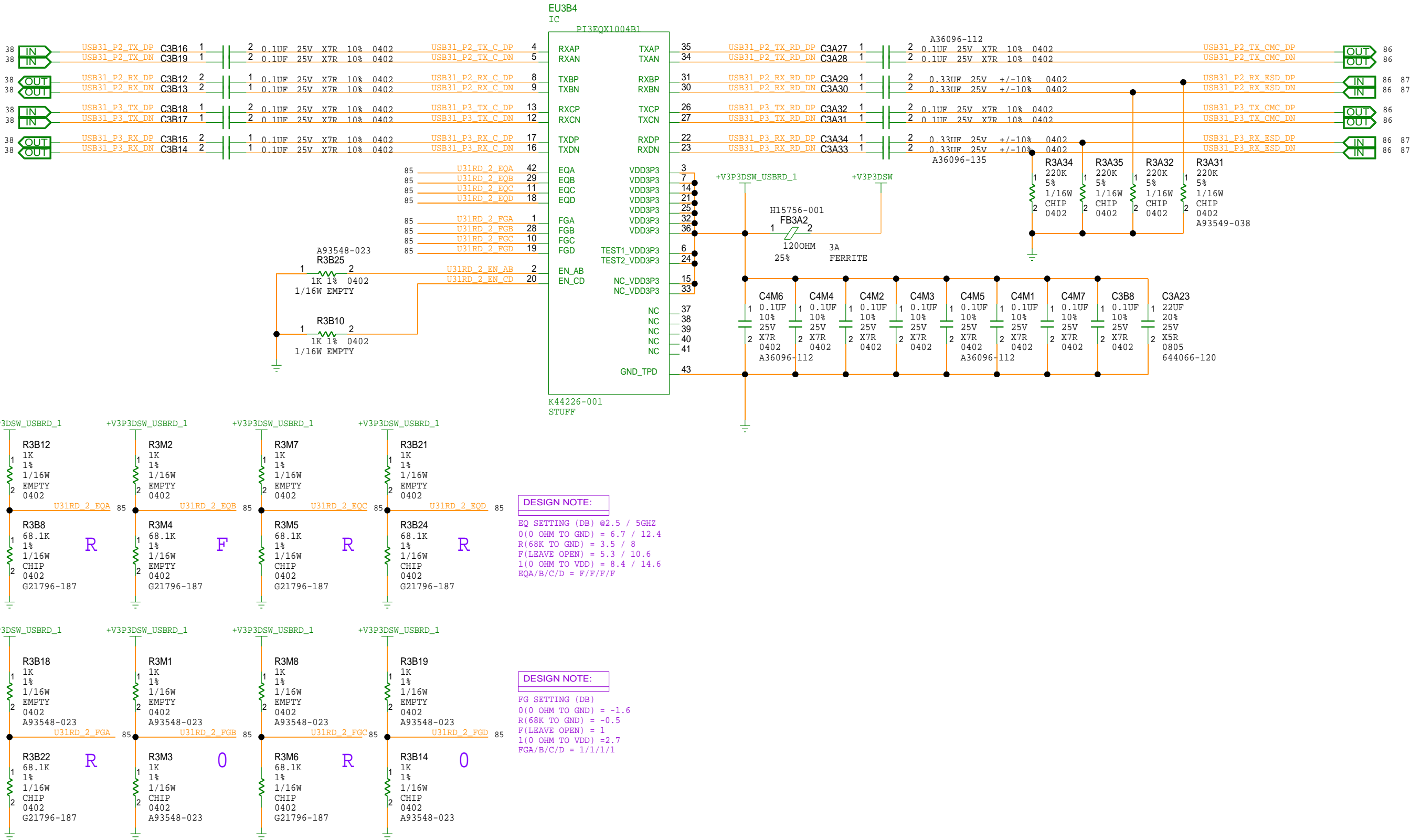
USB3.1 POWER FOR RJ45/USB STACK CONECTOR



USB3.1 TYPE-A BACK PANEL - REDRIVER  
PORT2/3

MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE\_TITLE=USB3.1 TYPE-A BACK PANEL 3&4 - REDRIVERS]

BPAGE DRAWING

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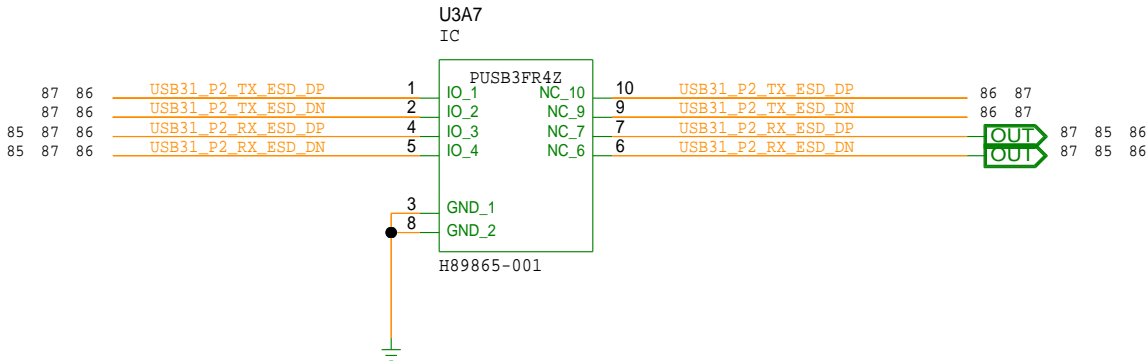
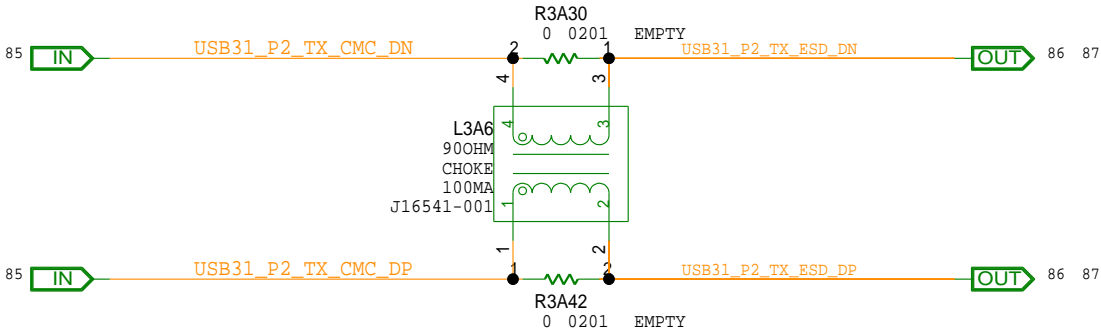
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CUSTOM TEXT BPAGE

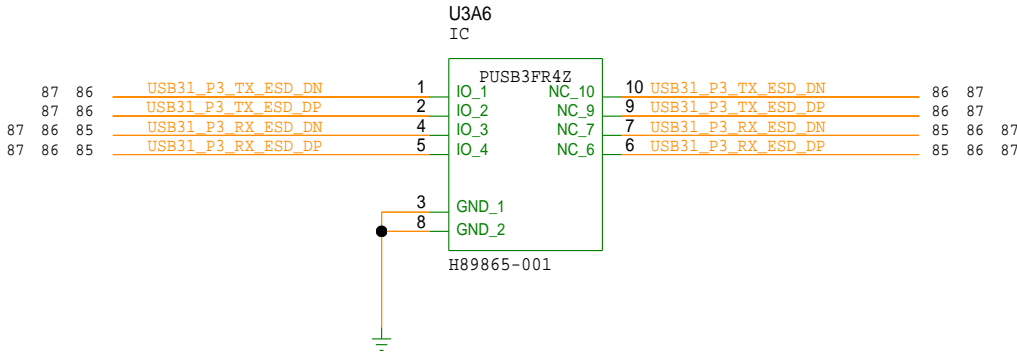
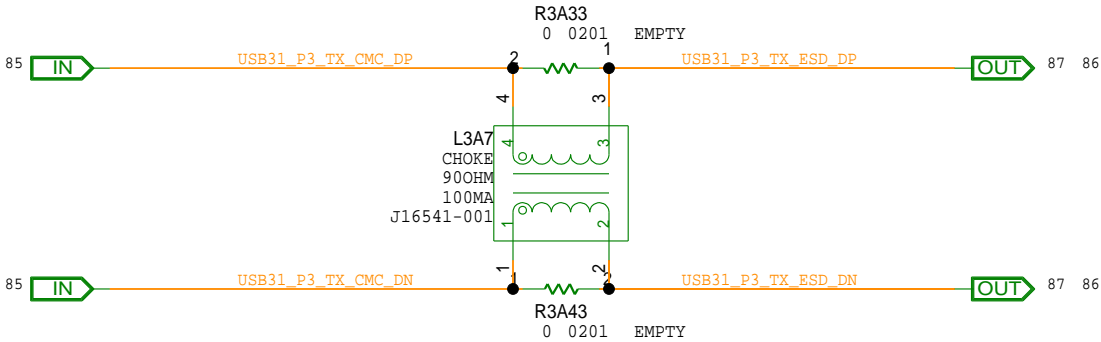
MODULE REV DETAILS

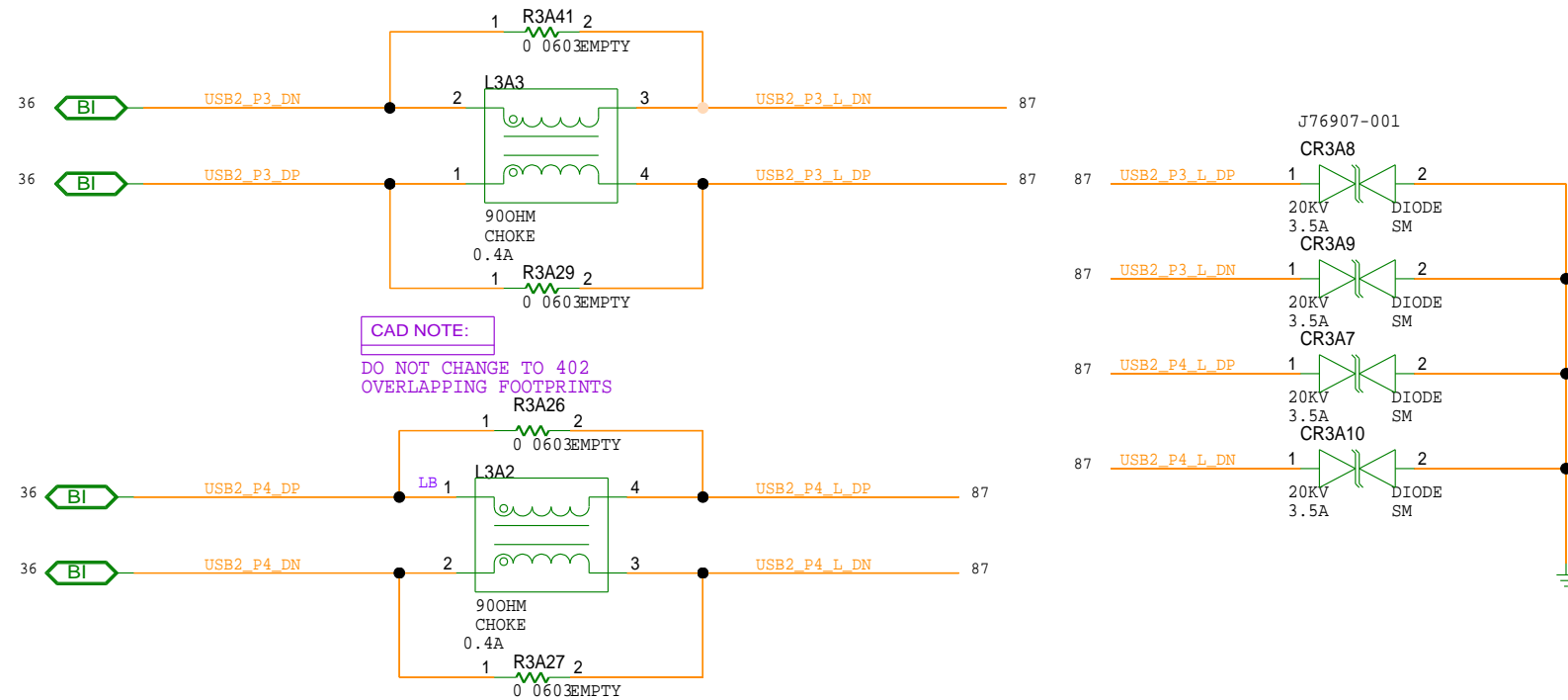
MODULE NAME	REV	DATE

USB3.1 TYPE-A BACK PANEL - CMC+ESD  
USB3.1 PORT2

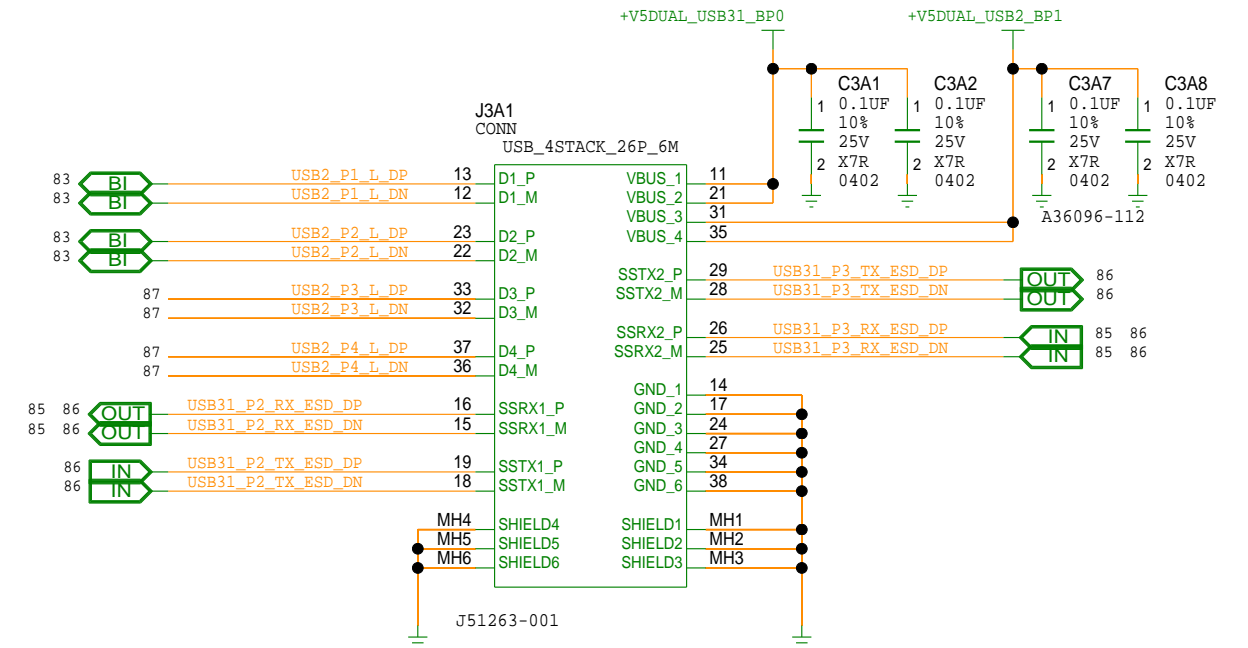


USB3.1 PORT3

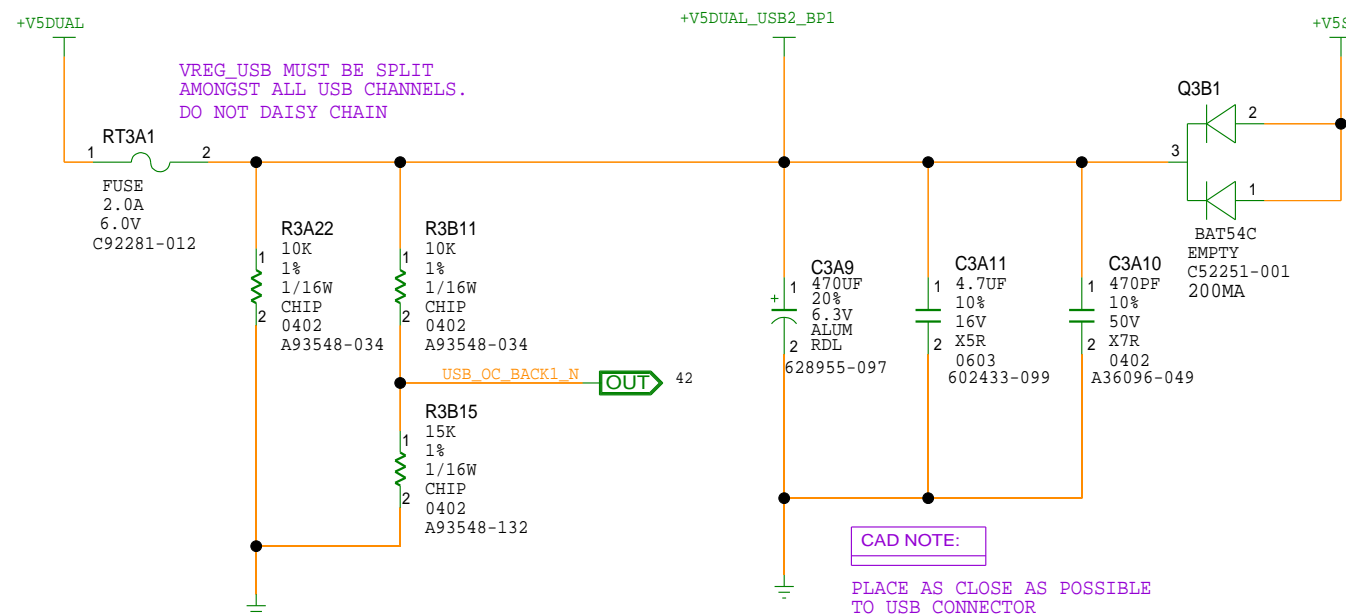




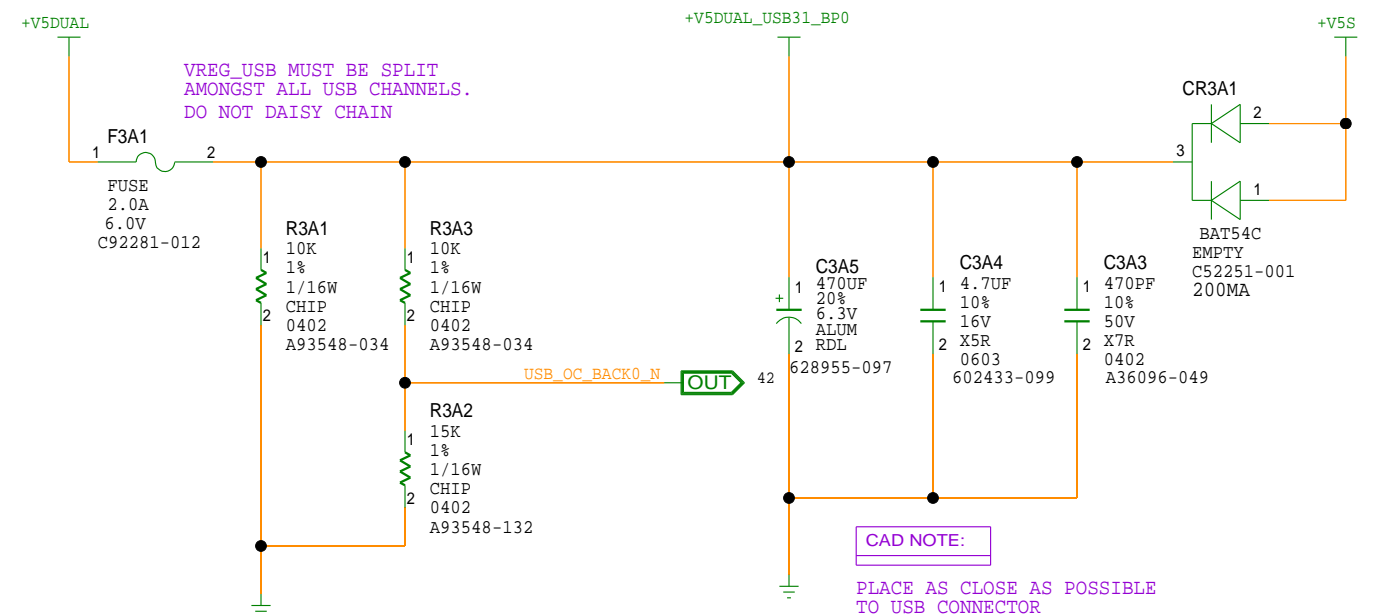
## USB31 STACK CONN



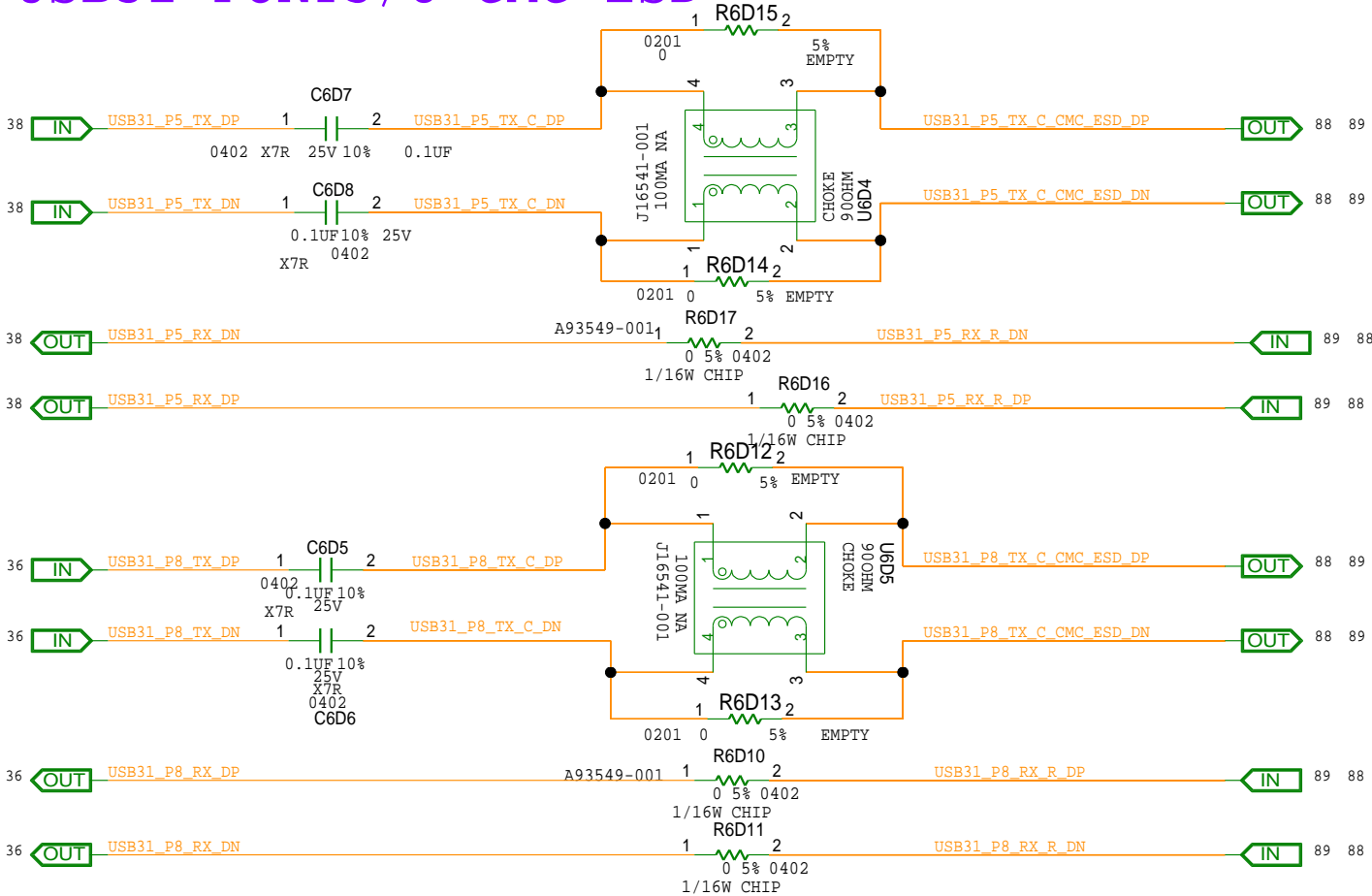
## USB POWER



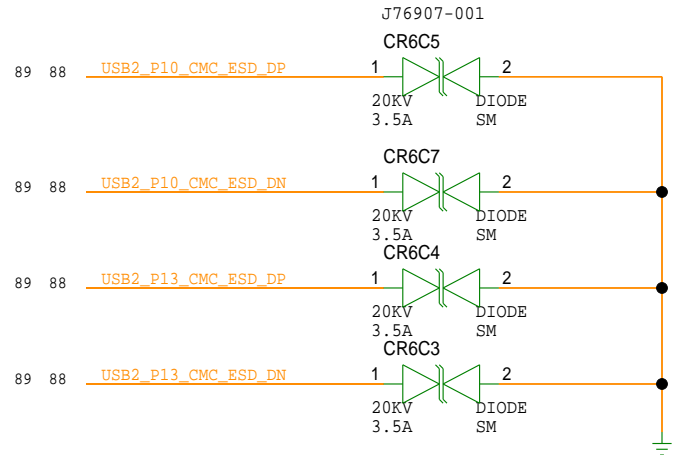
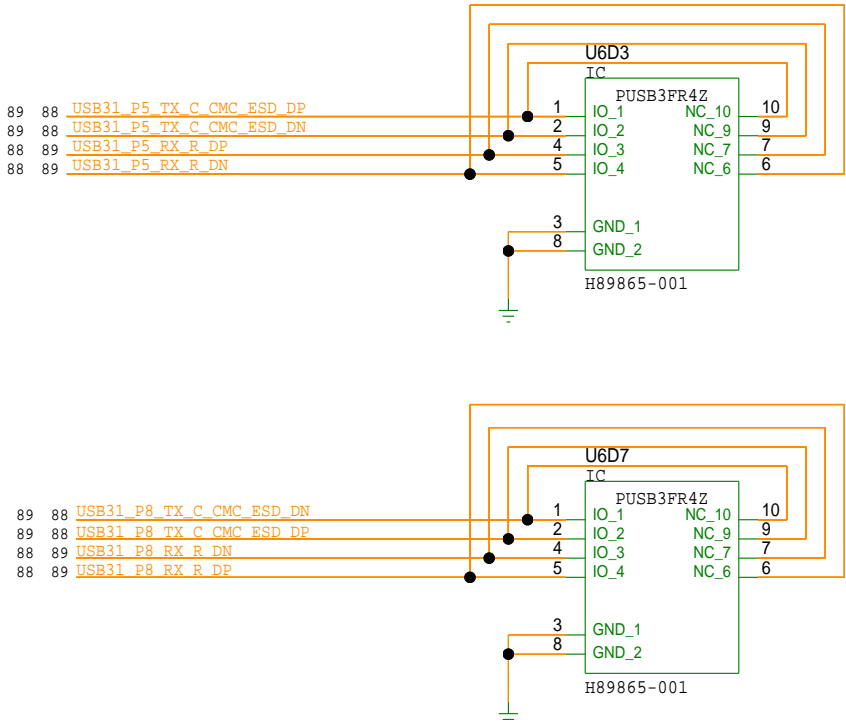
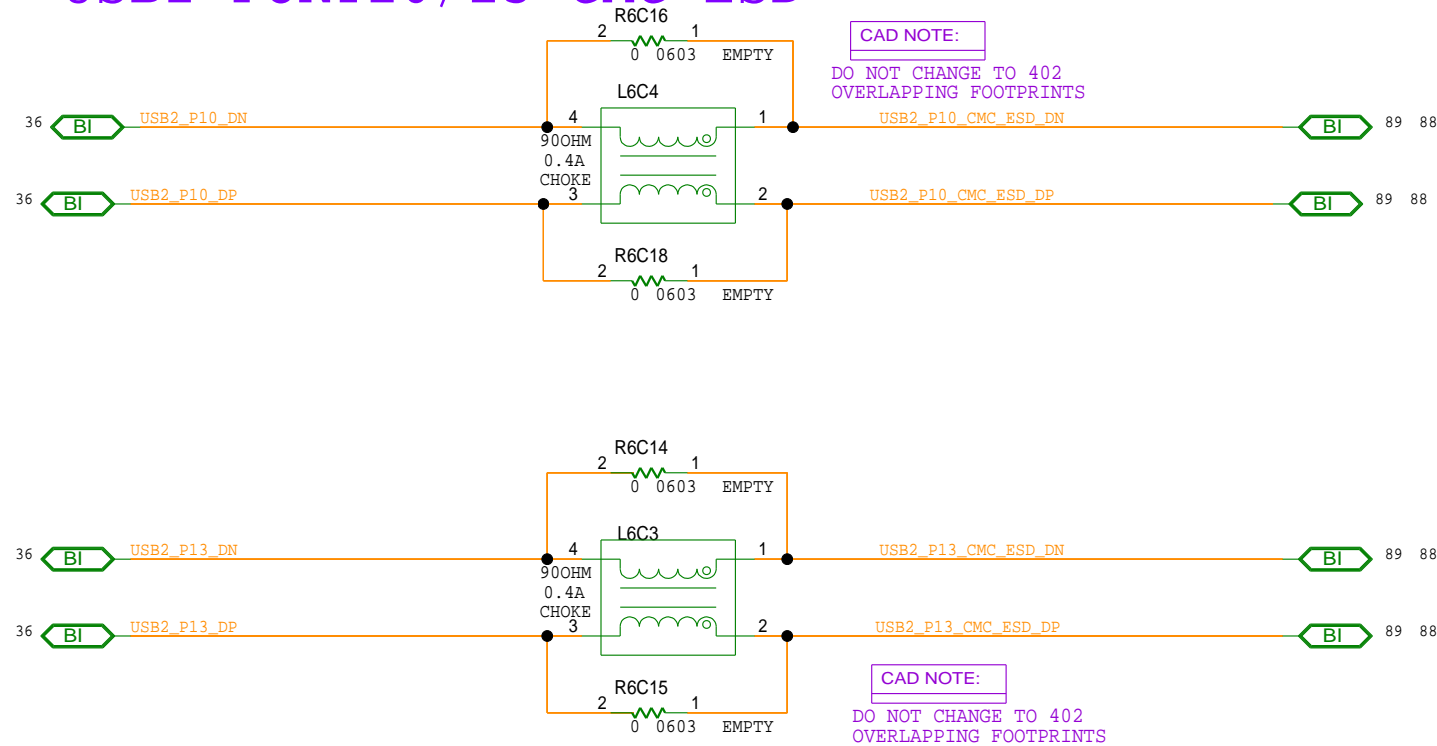
## USB POWER



USB31 PORT5/8 CMC+ESD



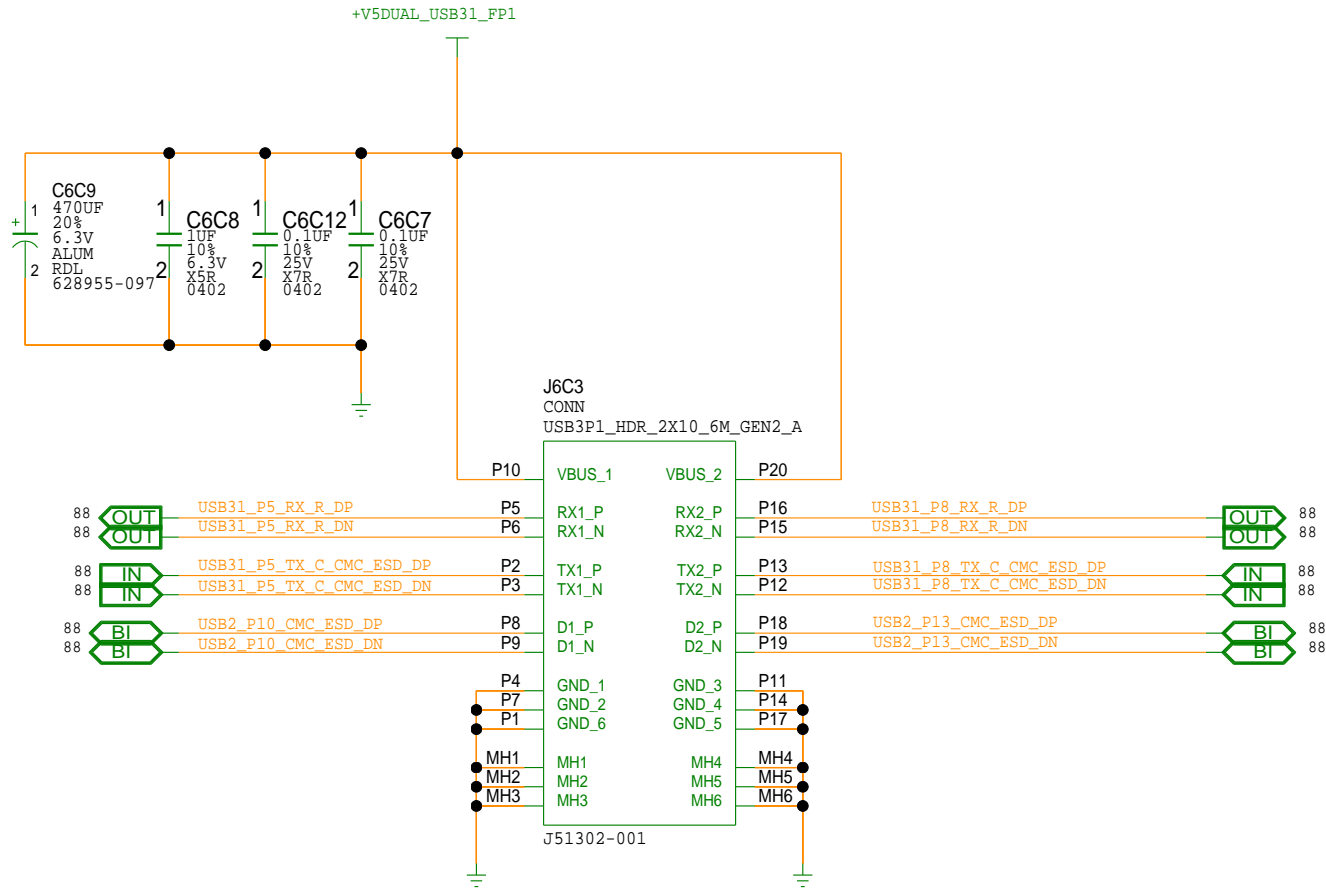
USB2 PORT10/13 CMC+ESD



MODULE REV DETAILS

MODULE NAME	REV	DATE

FRONT PANEL HEADER FOR TYPE-A



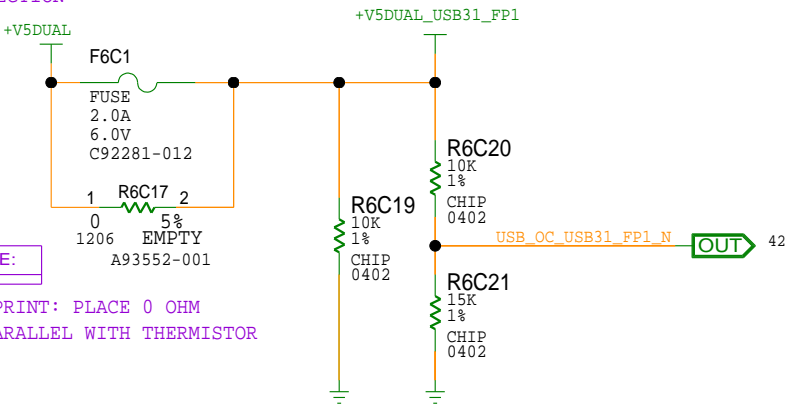
DESIGN NOTE:

STUFFING THE THERMISTOR ASSUMES FRONT PANEL CARD  
HAS NO FUSE AND DOES NOT PROVIDE OVER-CURRENT PROTECTION

FRONT PANEL POWER

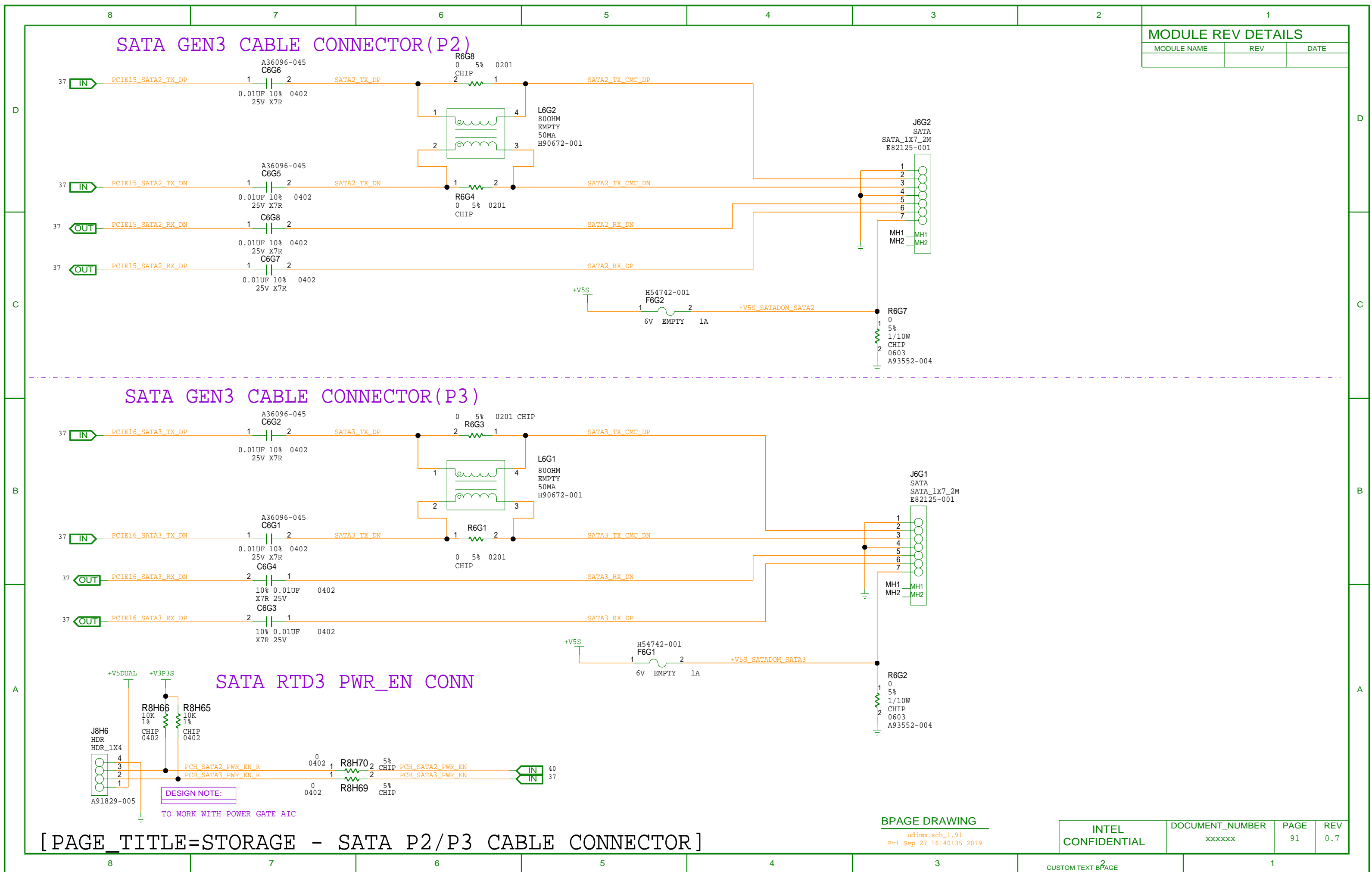
CAD NOTE:

DUAL FOOTPRINT: PLACE 0 OHM  
1206 IN PARALLEL WITH THERMISTOR







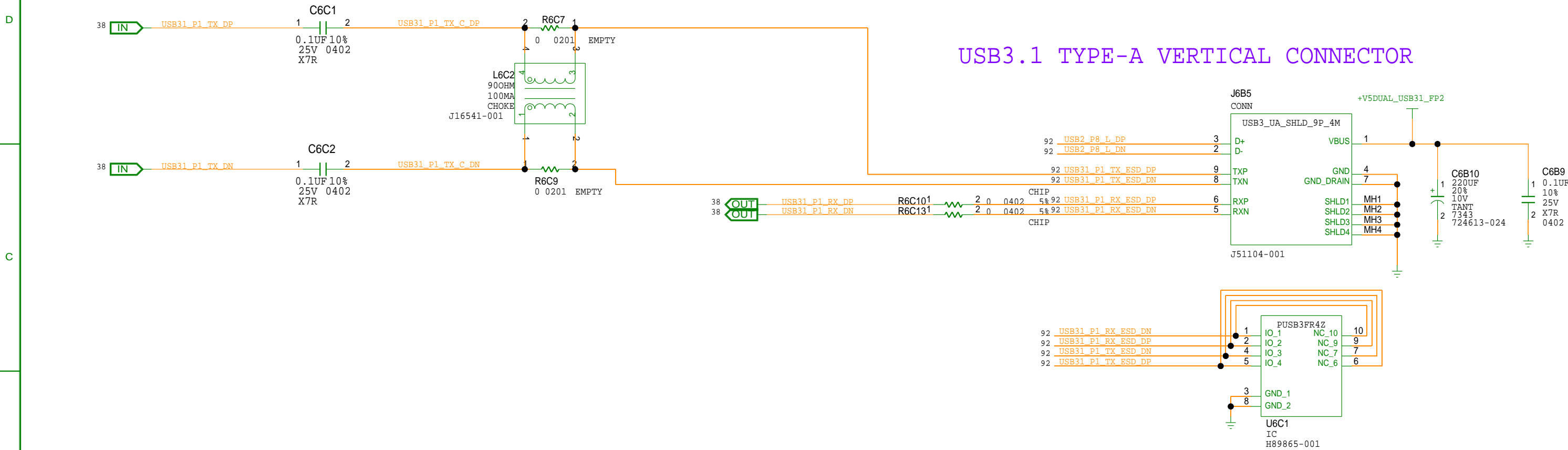


USB3.1 CMC+ESD  
PORT 1 - VERTICAL TYPE-A

MODULE REV DETAILS

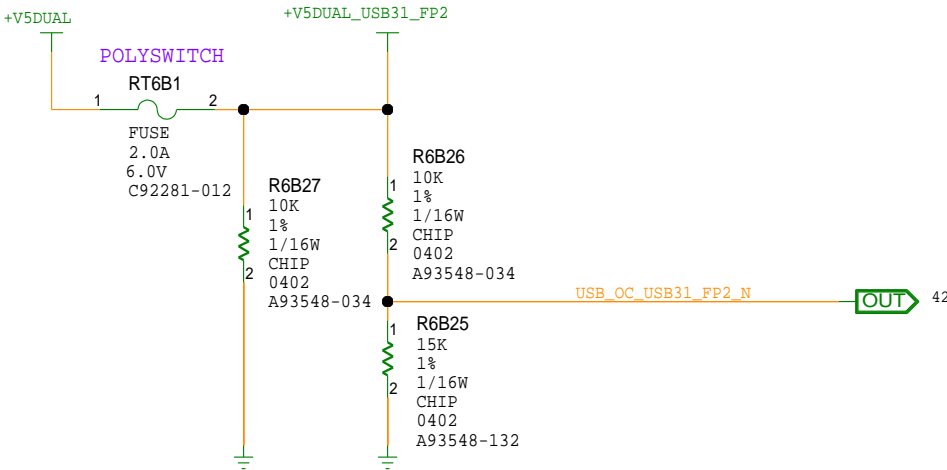
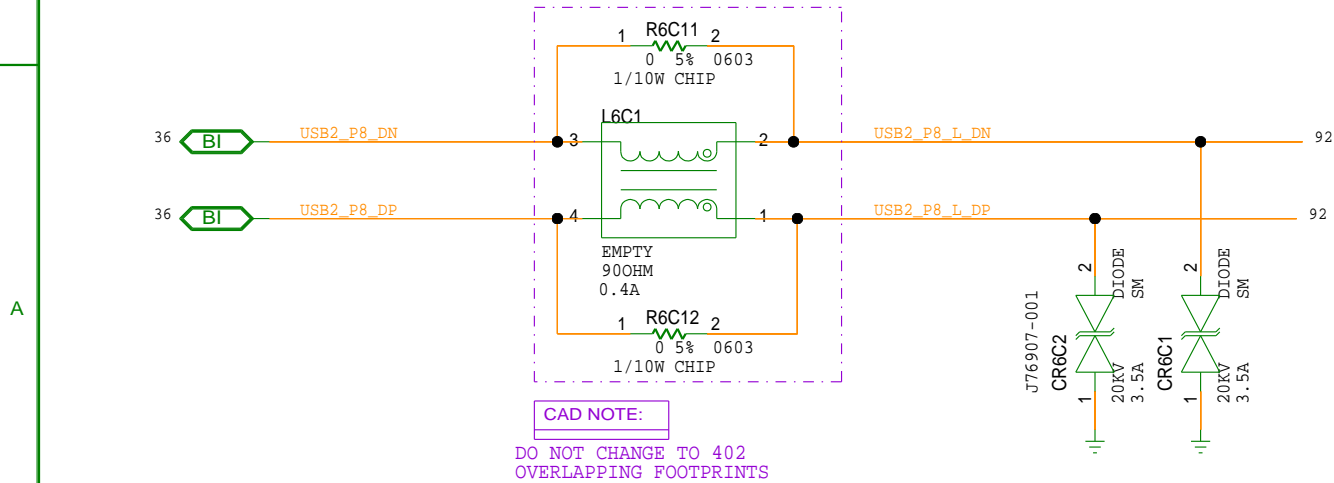
MODULE NAME	REV	DATE

USB3.1 TYPE-A VERTICAL CONNECTOR



USB2.0 CMC+ESD  
PORT 8 - VERTICAL TYPE-A

USB POWER -VERTICAL TYPE-A



[PAGE\_TITLE = USB3.1 TYPE-A VERTICAL]

BPAGE DRAWING

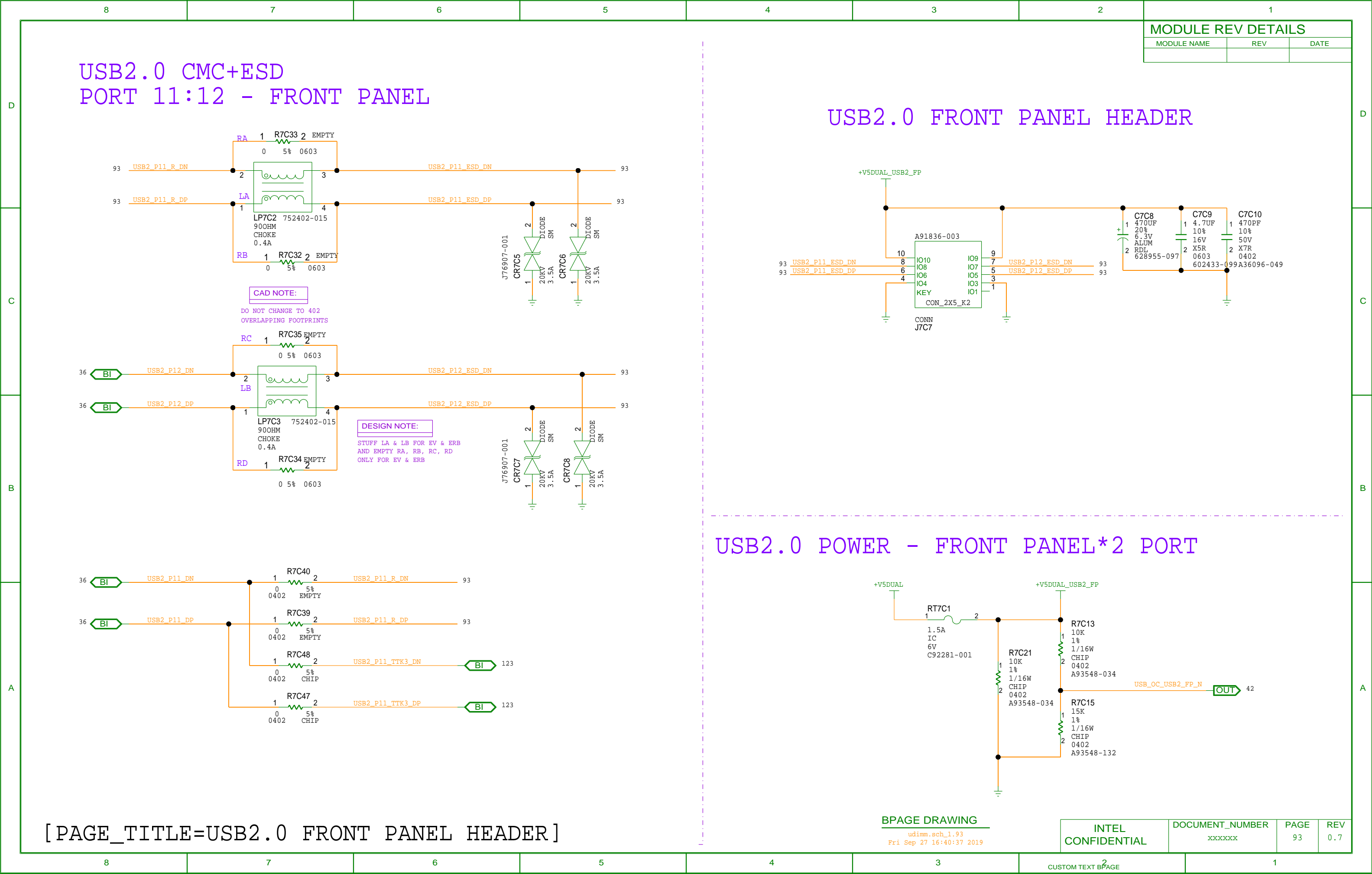
udimm.sch\_1.92  
Fri Sep 27 16:40:36 2019

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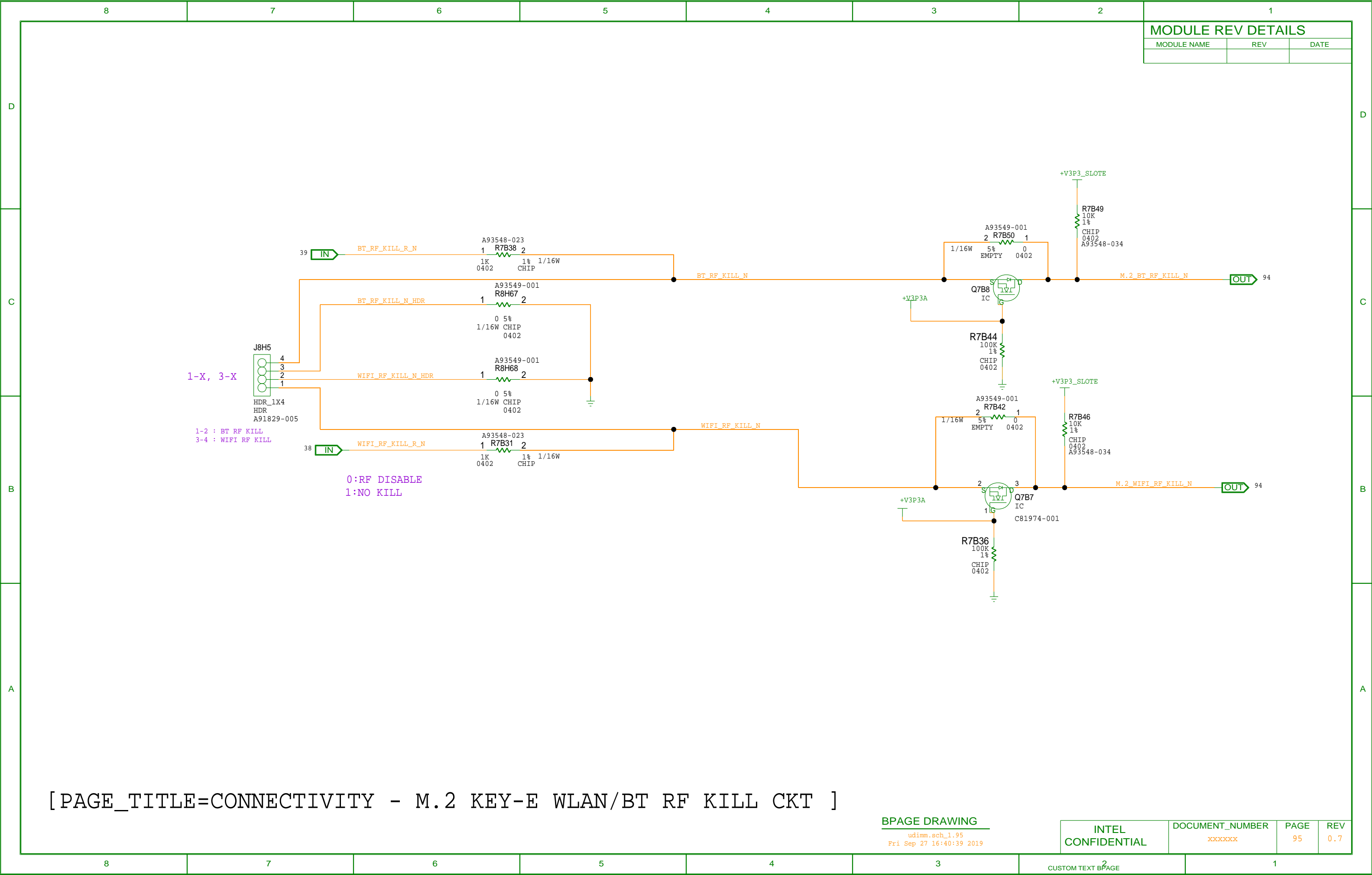
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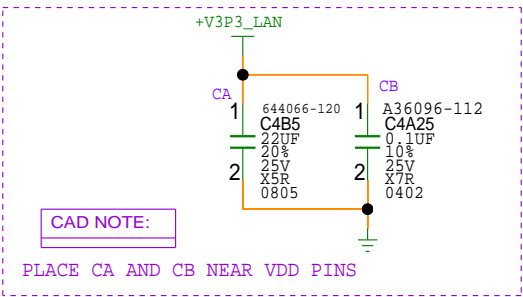






[ PAGE\_TITLE=CONNECTIVITY - M.2 KEY-E WLAN/BT RF KILL CKT ]

MODULE NAME	REV	DATE



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## D



## B



PLACE THE ESD PROTECTION DIODE (ESD1014) CLOSE TO LAN CONNECTOR.

## D



## B



8	7	6	5	4	3	CUSTOM TEXT PAGE	1
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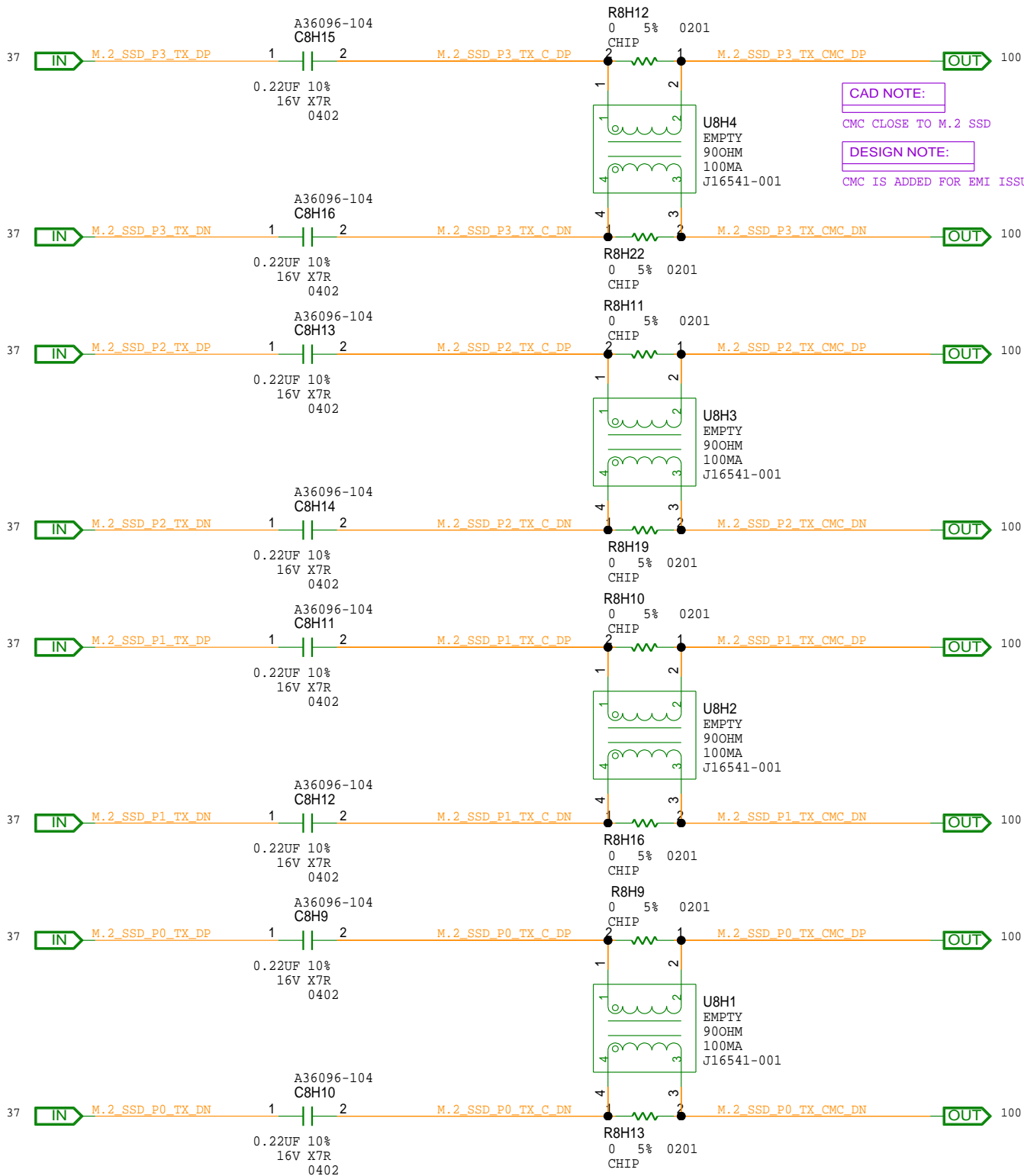
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MODULE REV DETAILS

MODULE NAME	REV	DATE

AC CAP + CMC FOR M.2 SOCKET-3 SSD



CAD NOTE:

CMC CLOSE TO M.2 SSD

DESIGN NOTE:

CMC IS ADDED FOR EMI ISSUE

BPAGE DRAWING

udimm.sch.1.99  
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CONFIDENTIAL

DOCUMENT\_NUMBER

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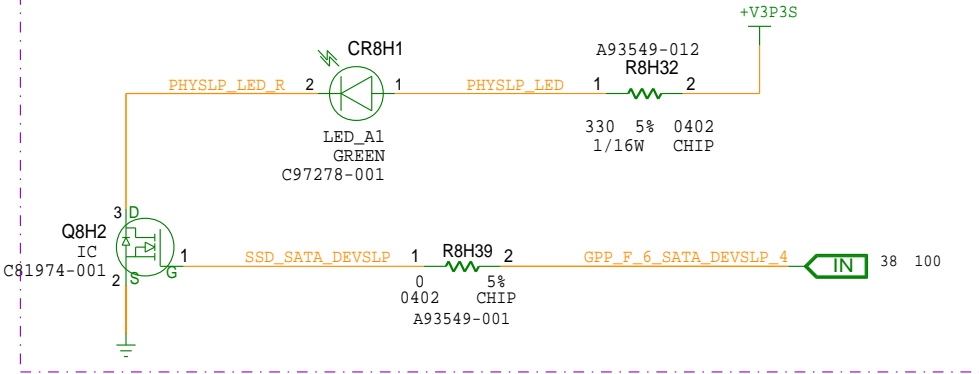
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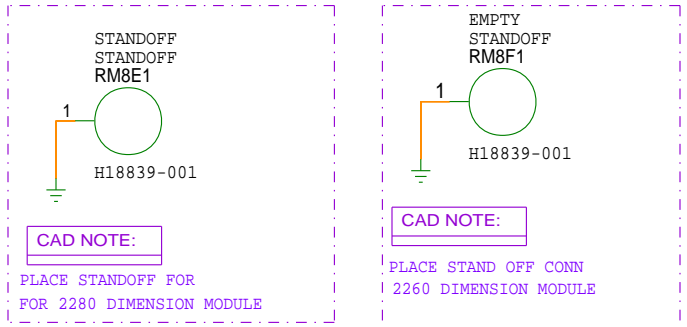
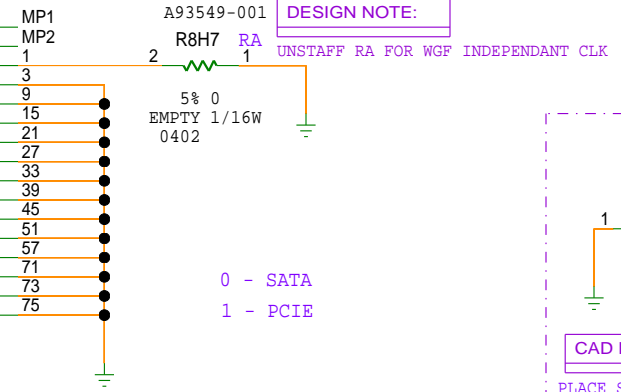
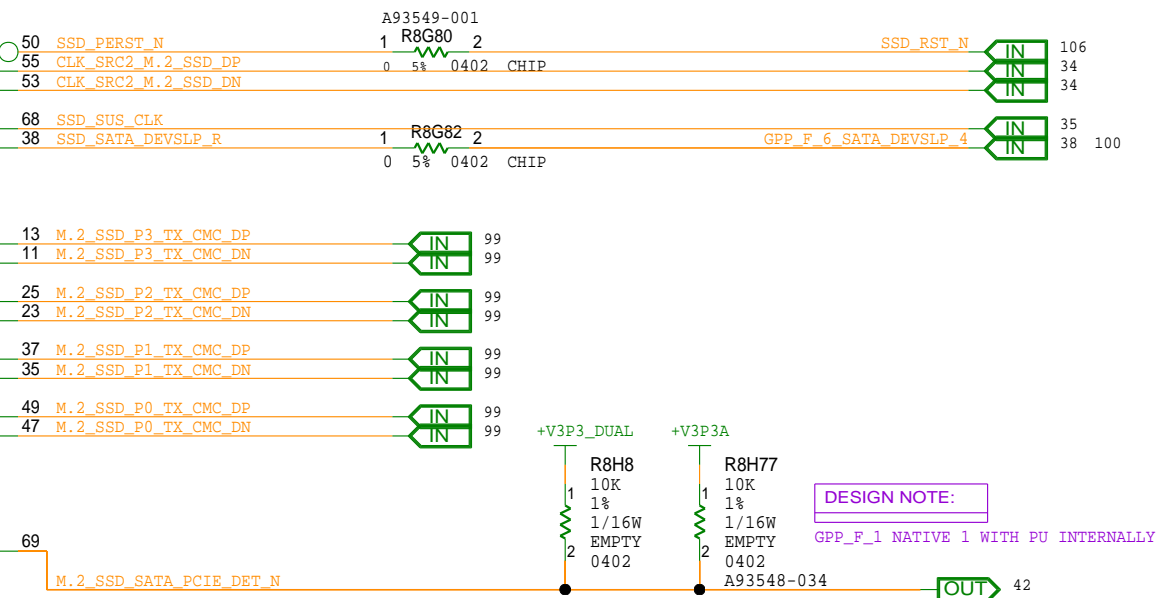
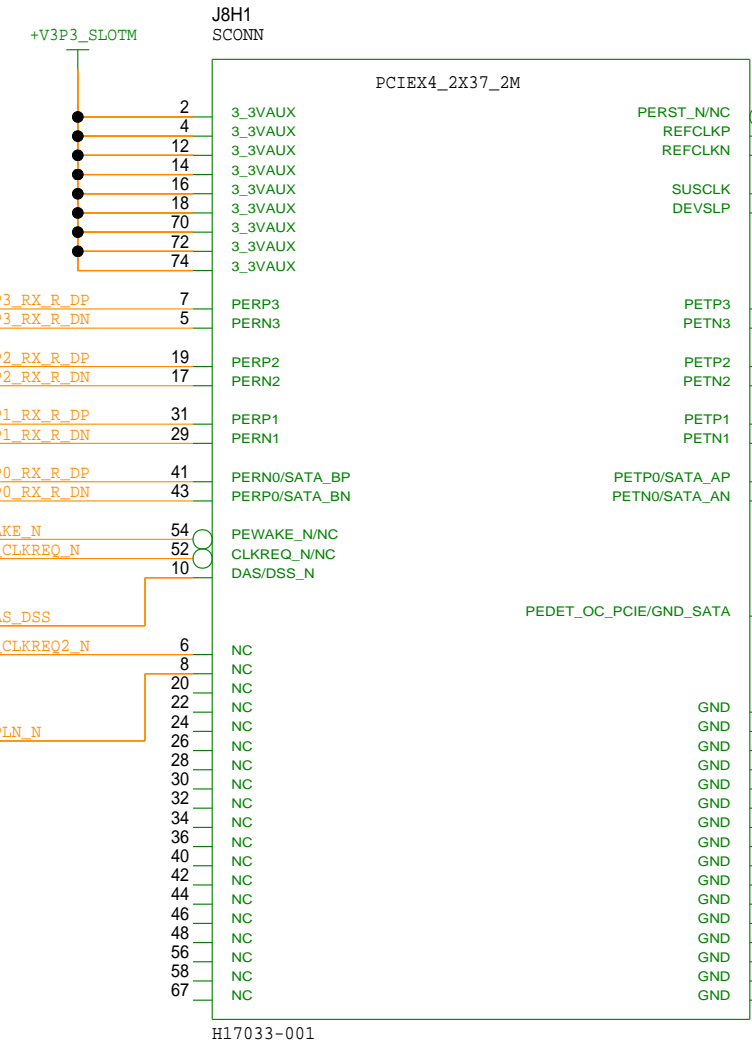
MODULE REV DETAILS

MODULE NAME	REV	DATE

SATA DEVSLP LED FOR M.2 SSD



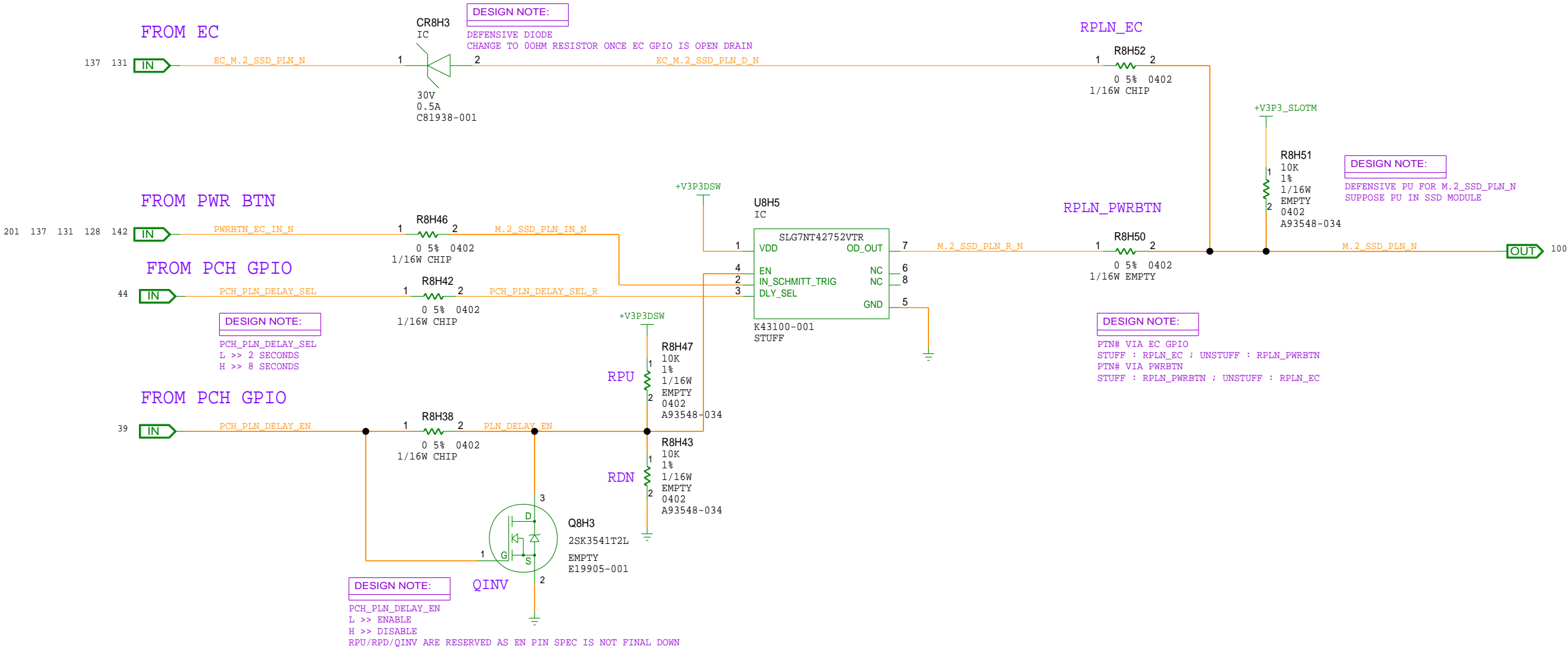
M.2 SOCKET-3 SSD  
8.2MM HEIGHT CONNECTOR



MODULE REV DETAILS

MODULE NAME	REV	DATE
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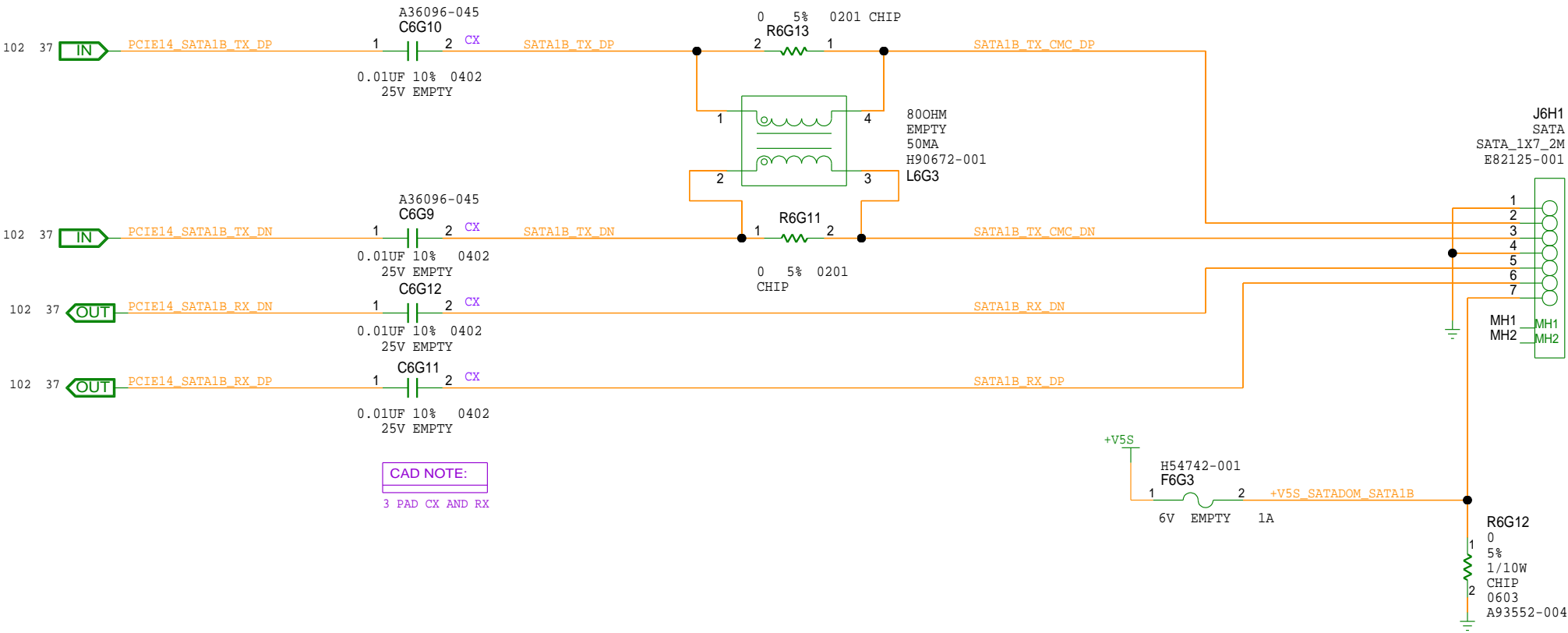
M.2 SOCKET-3 SSD PLN# CIRCUIT



SATA GEN3 CABLE CONNECTOR(P1B)

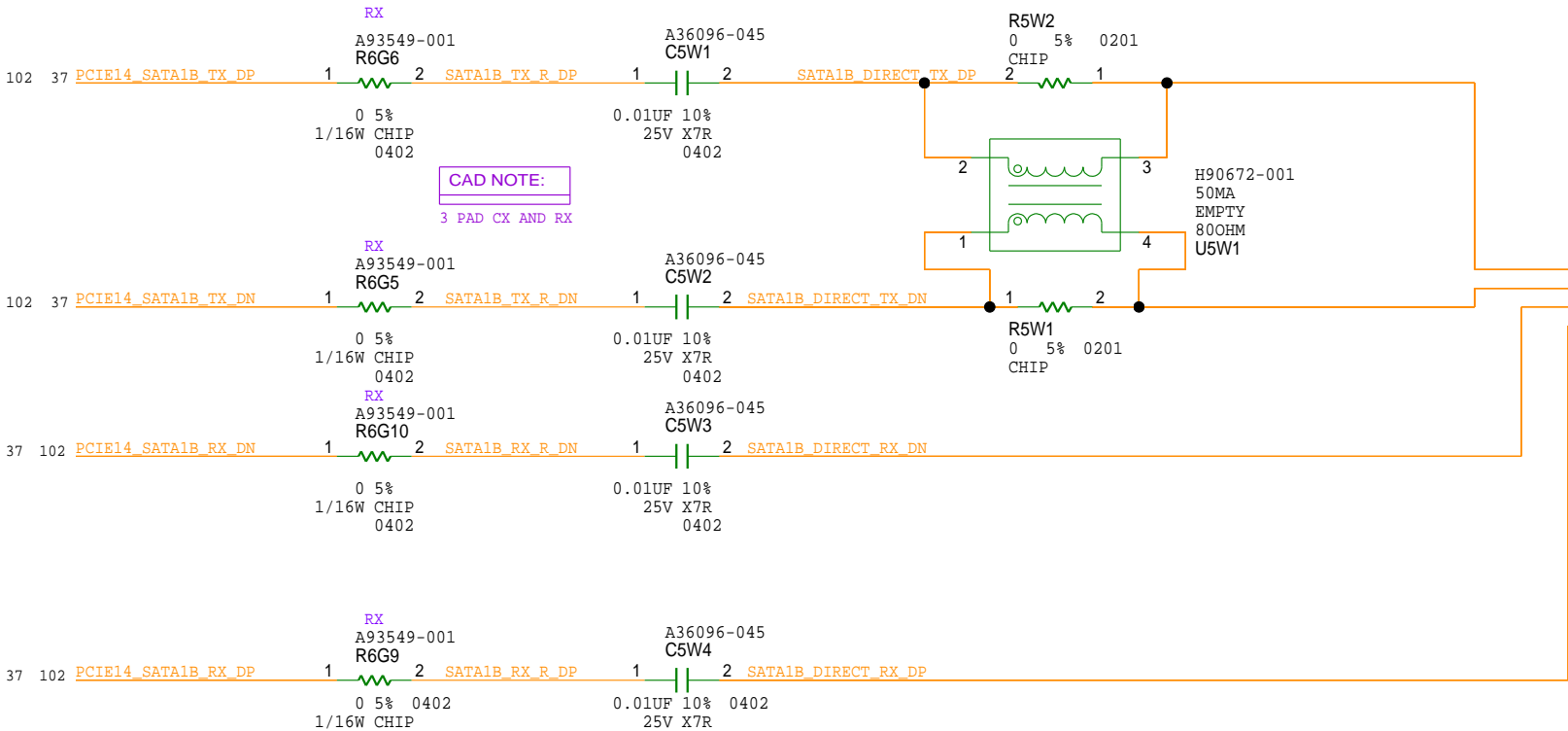
MODULE REV DETAILS

MODULE NAME	REV	DATE

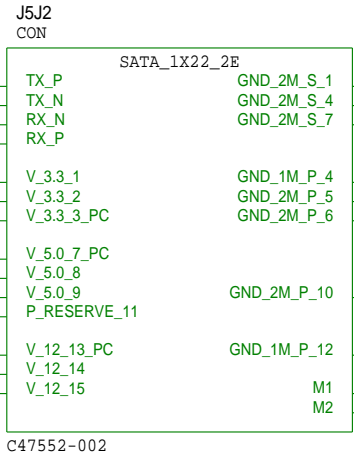
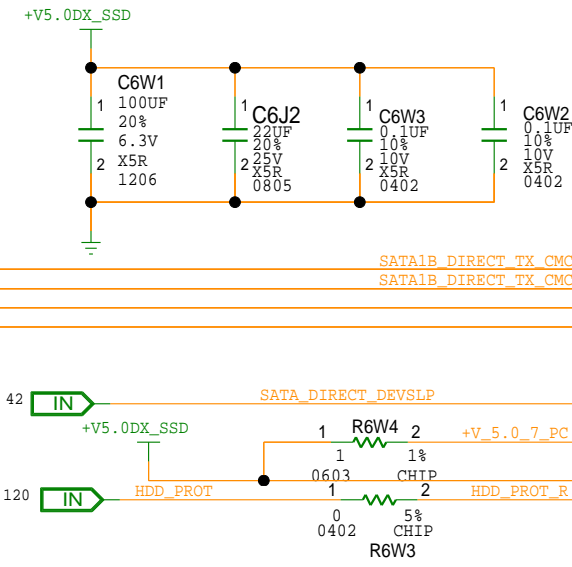


CAD NOTE:  
3 PAD CX AND RX

SATA GEN3 DIRECT CONNECTOR (P1B)



CAD NOTE:  
3 PAD CX AND RX



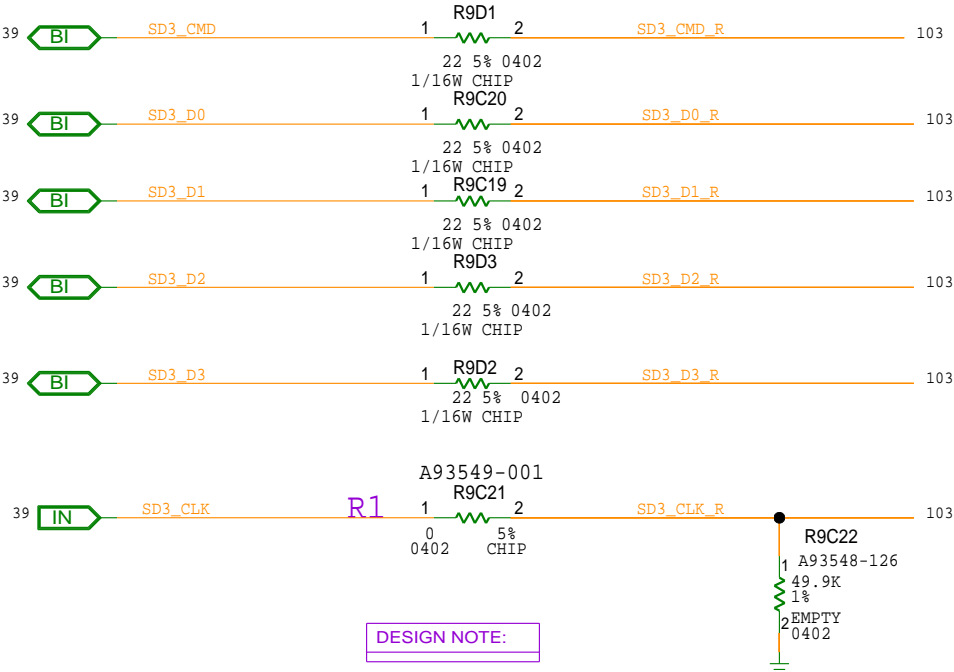
STORAGE - SD CONNECTOR

MODULE REV DETAILS

MODULE NAME	REV	DATE

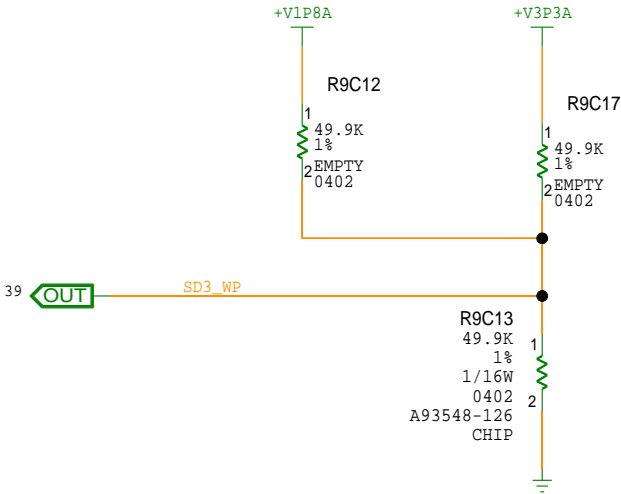
CAD NOTE:

PLACE SERIES RESISTORS CLOSE TO CONNECTOR WITHIN 12.7MM

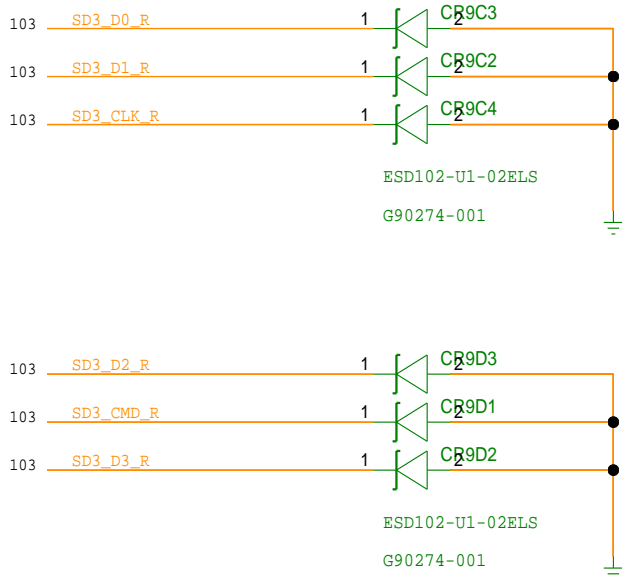


DESIGN NOTE:

R1 IS FOR DEBUG PURPOSE. SERIES RESISTOR ON SD3\_CLK IS NOT REQUIRED



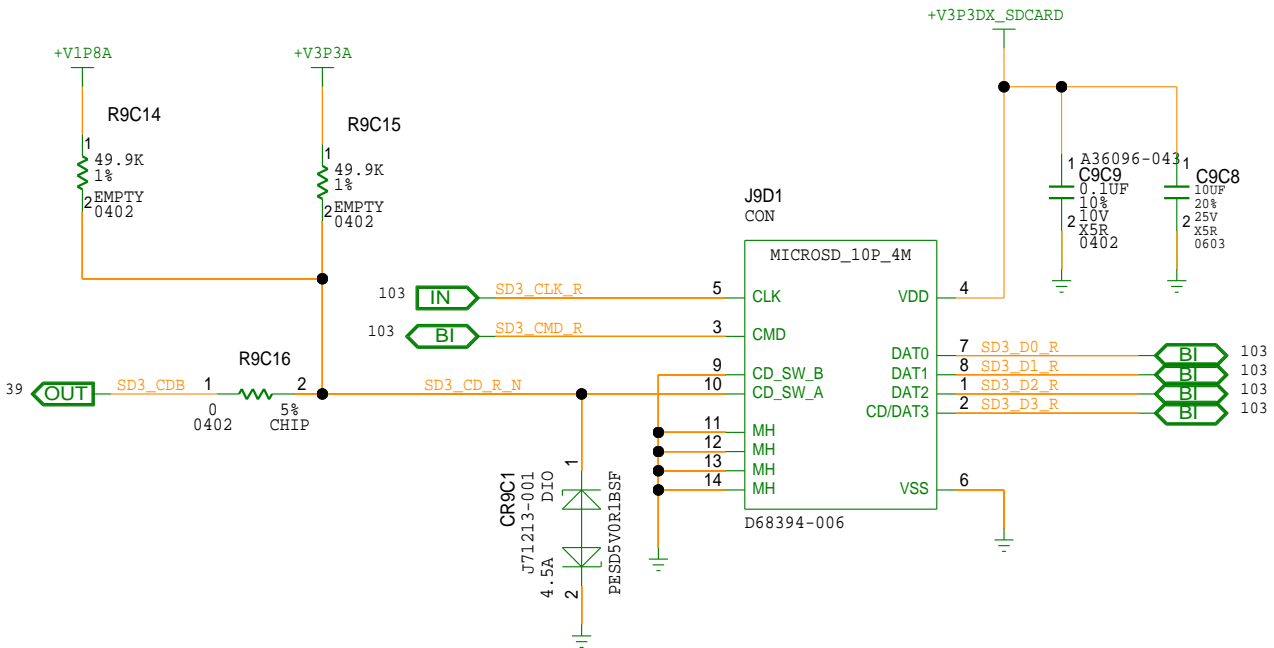
ESD PROTECTION DIODE

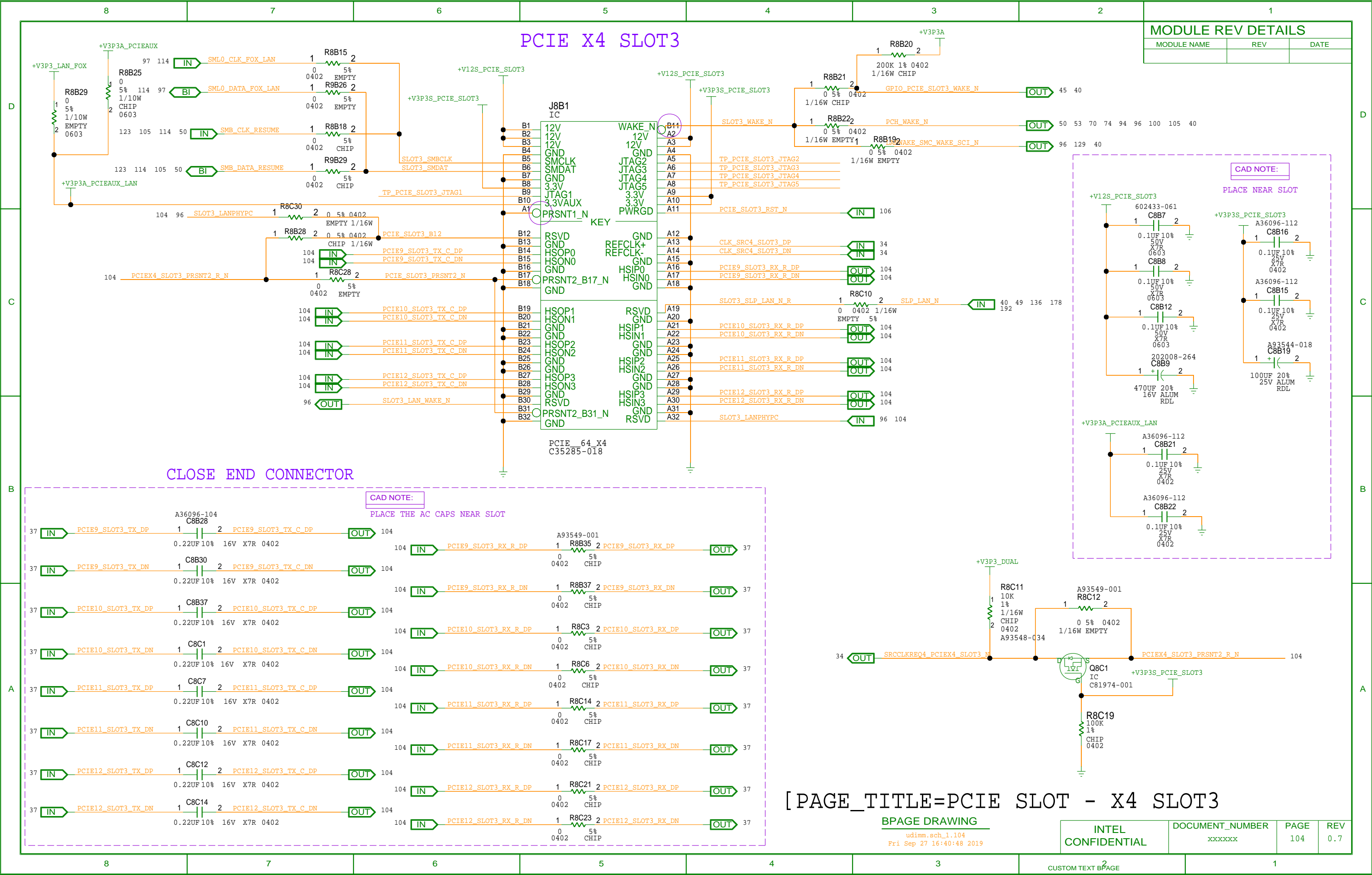


DESIGN NOTE:

ESD3V3XU1US COMPLIANCE

MICRO SD3.0 CARD CONNECTOR





[PAGE\_TITLE=PCIE SLOT - X4 SLOT3]

BPAGE DRAWING

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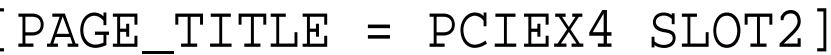
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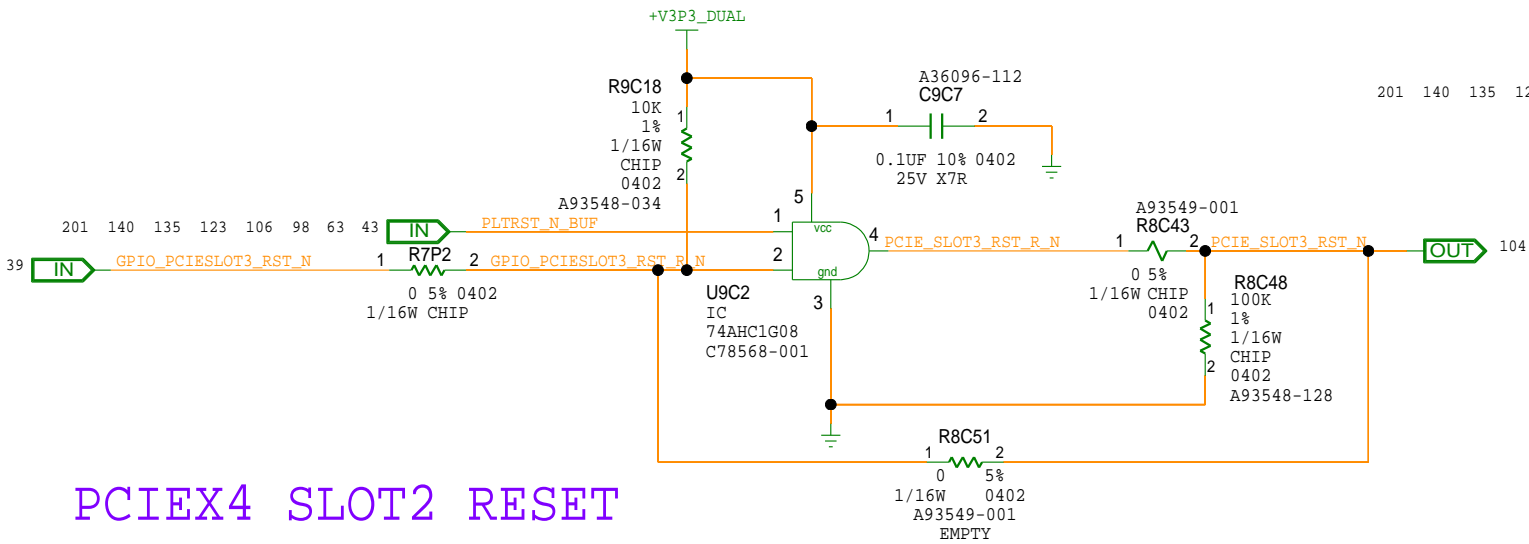




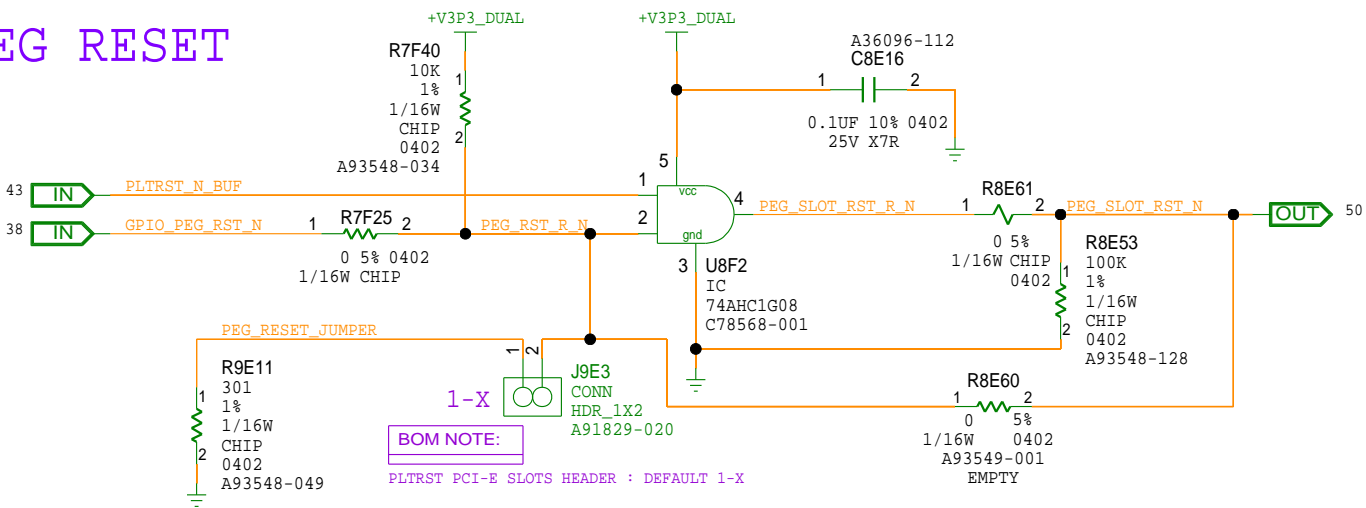
MODULE REV DETAILS

MODULE NAME	REV	DATE

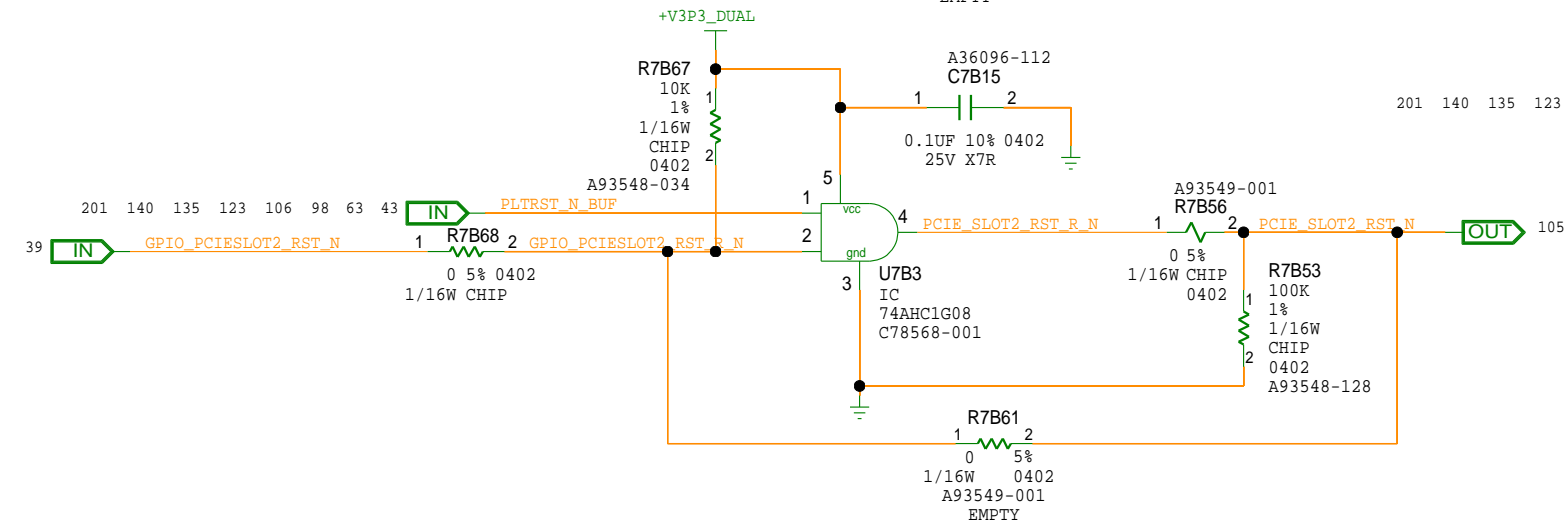
PCIEX4 SLOT3 RESET



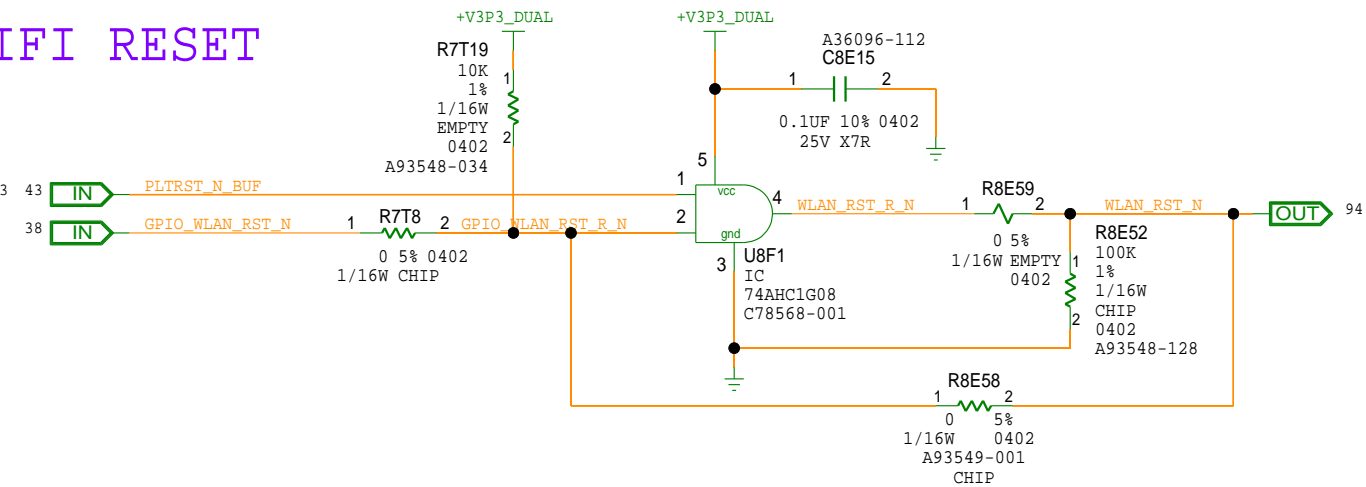
PEG RESET



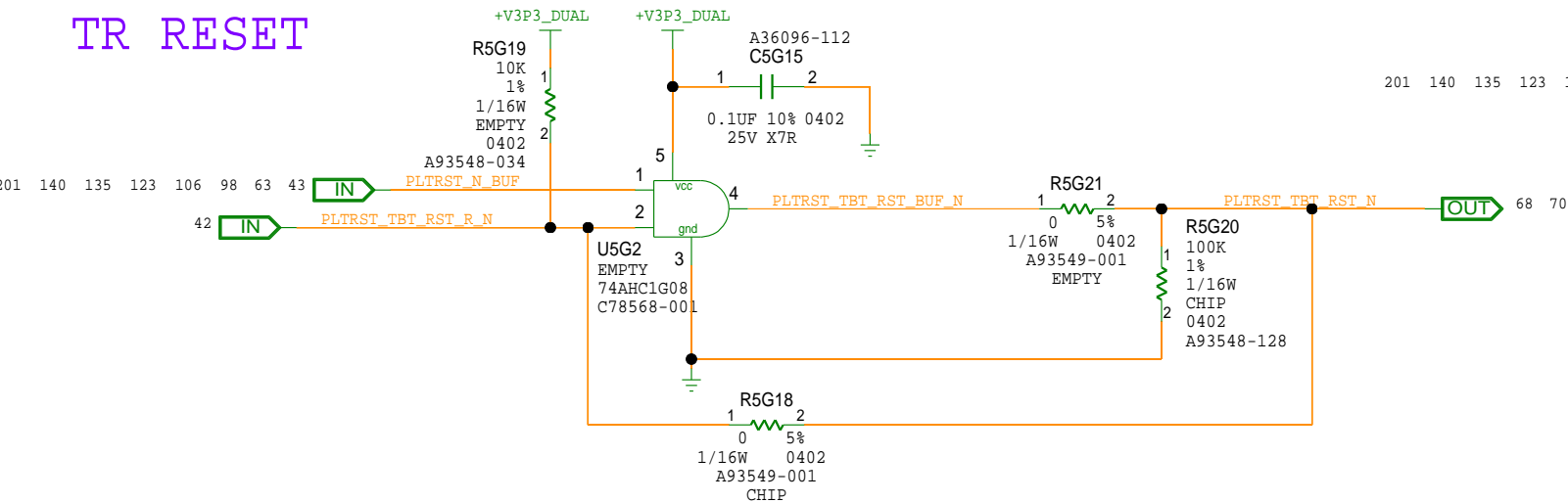
PCIEX4 SLOT2 RESET



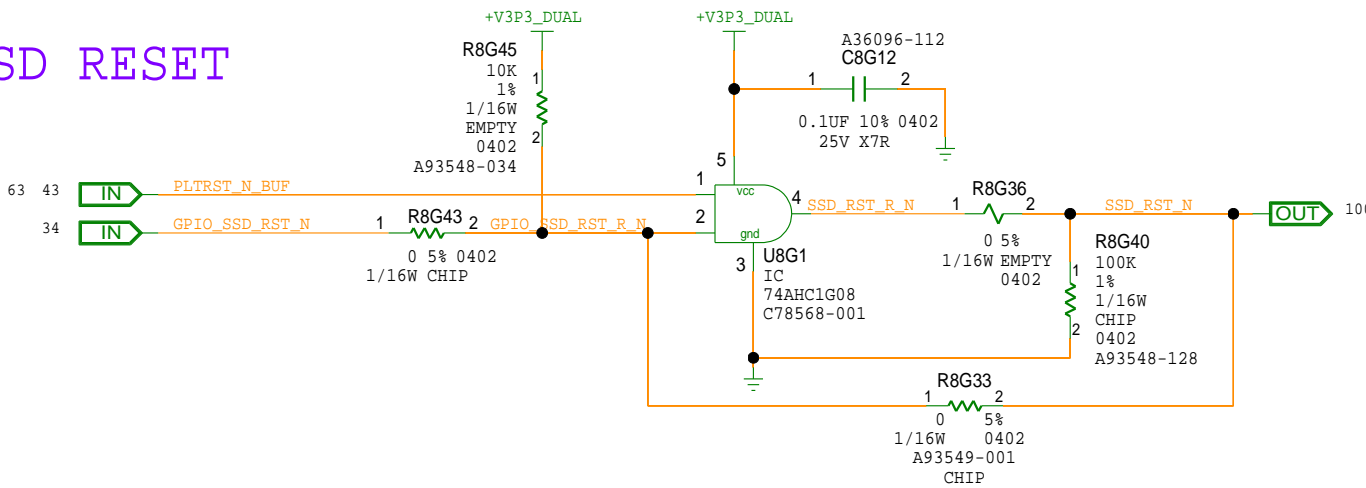
WIFI RESET



TR RESET



SSD RESET



[PAGE\_TITLE=PCIE RESET LOGIC]

BPAGE DRAWING

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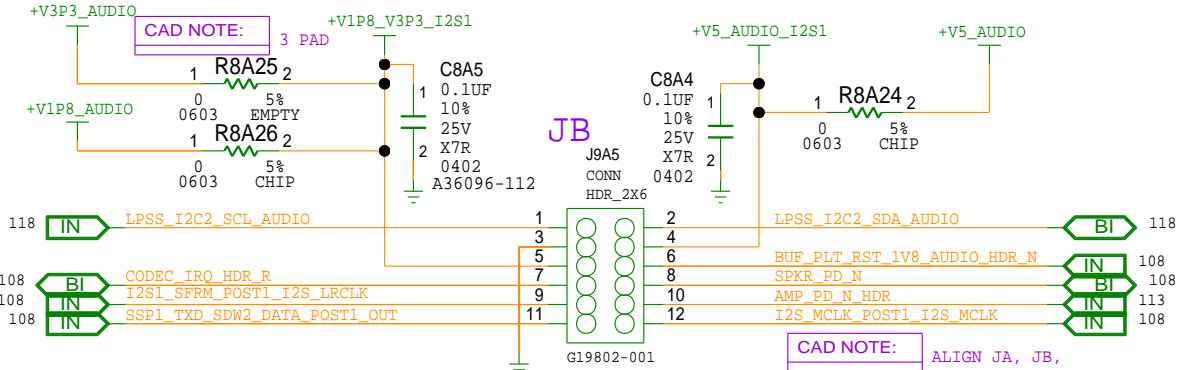
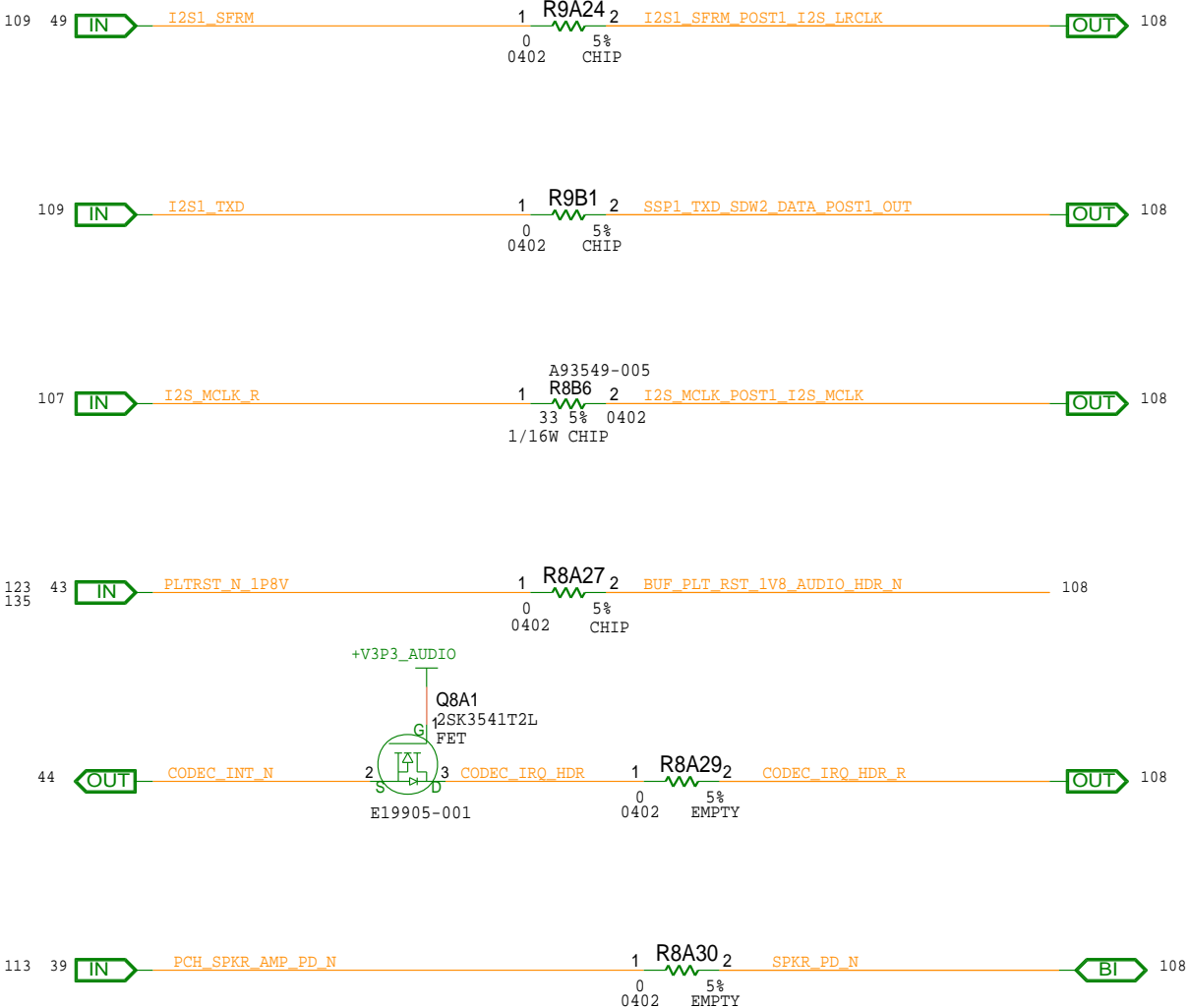
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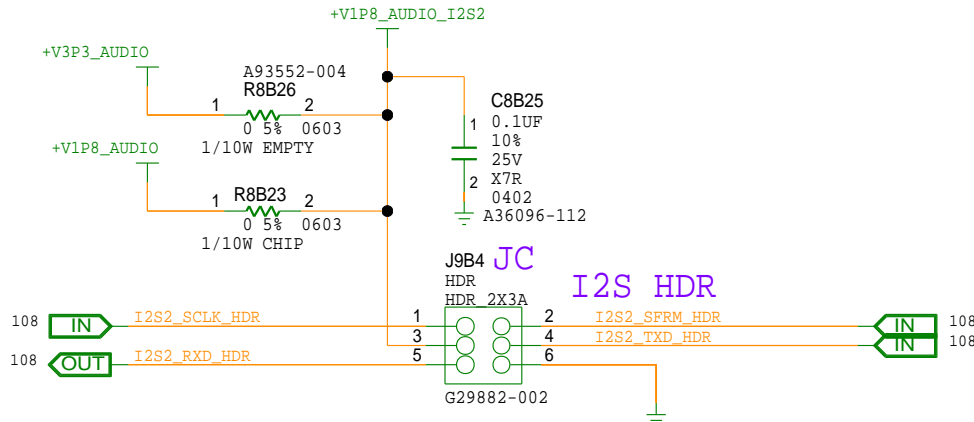
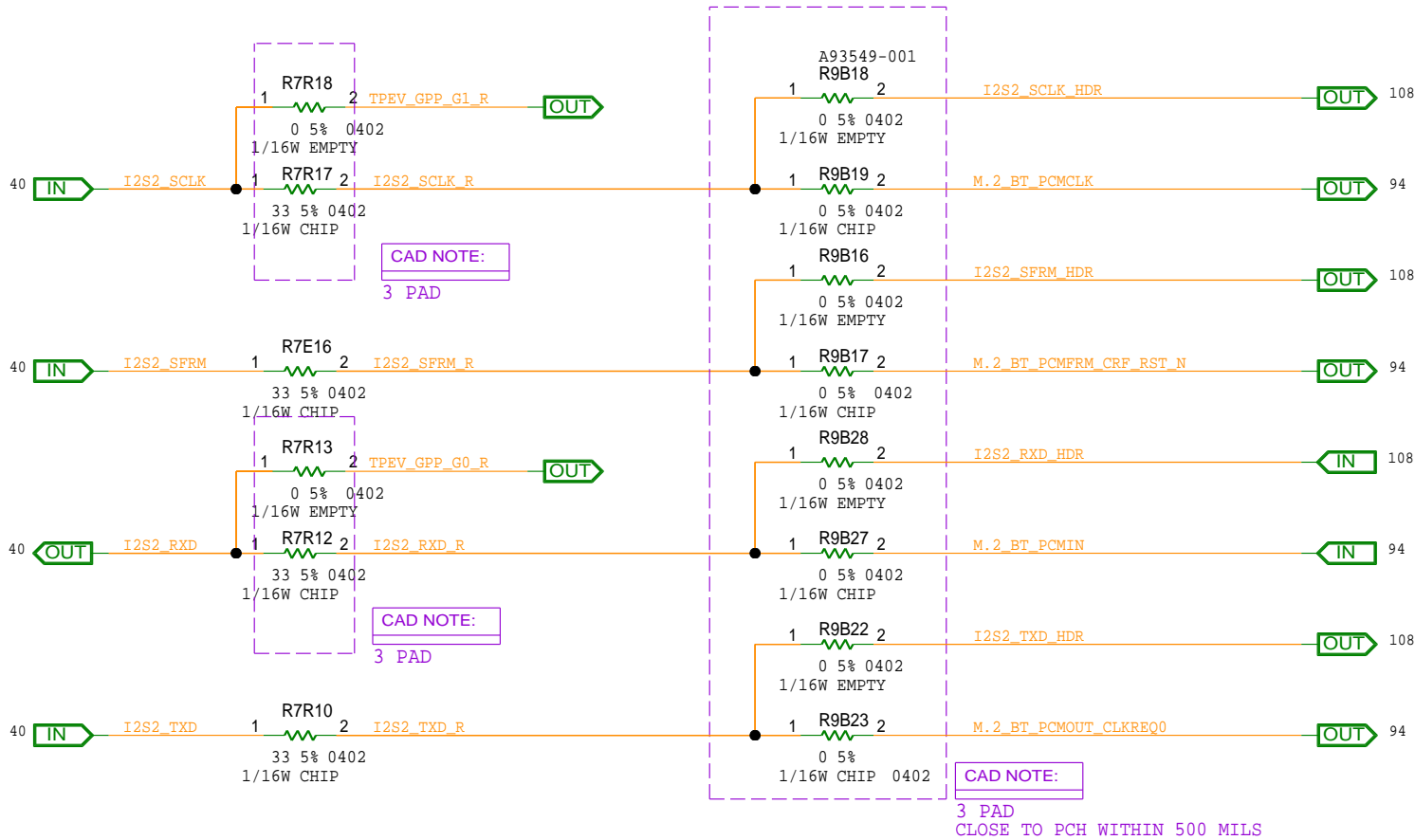
MODULE REV DETAILS

MODULE NAME	REV	DATE

PCH I2S1 TO HDR



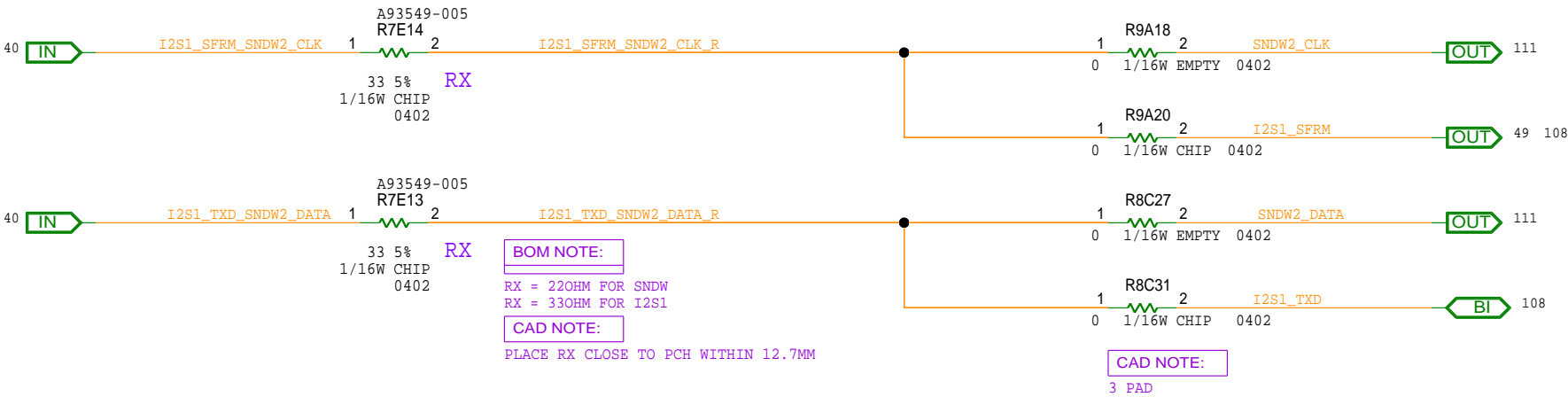
I2S2 OPTIONS TO M.2 BT OR HDR



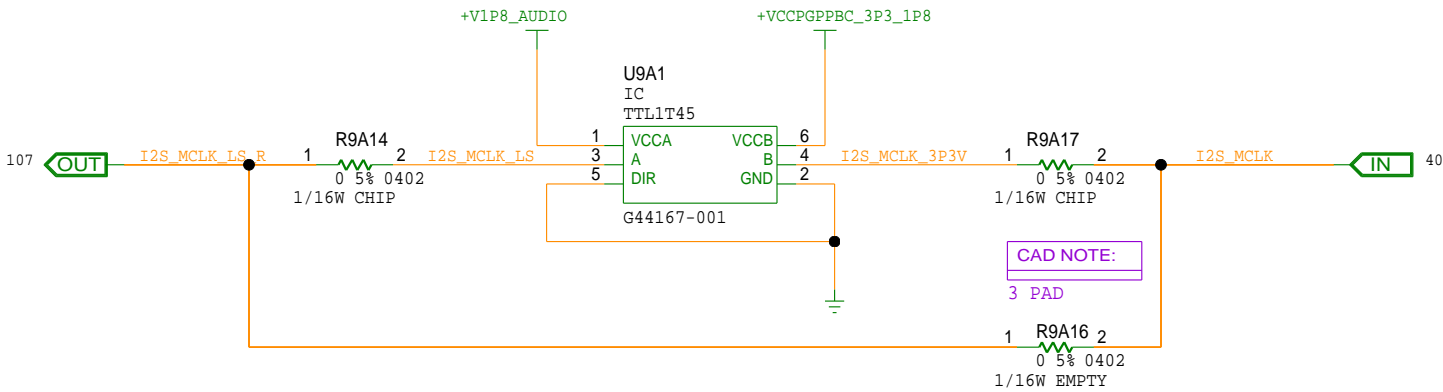
MODULE REV DETAILS

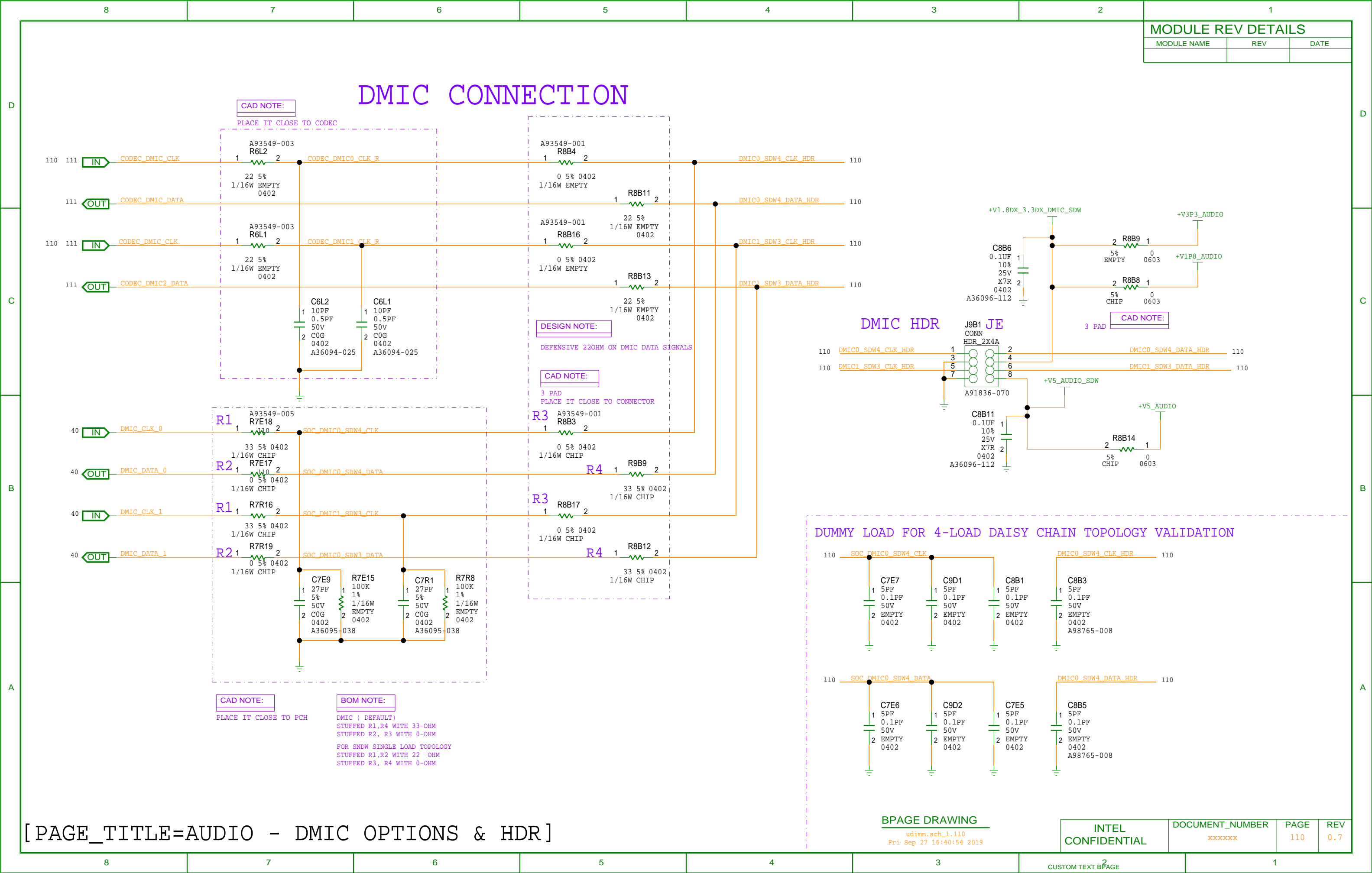
MODULE NAME	REV	DATE
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SNDW2/I2S1 1 LOAD TOPOLOGY

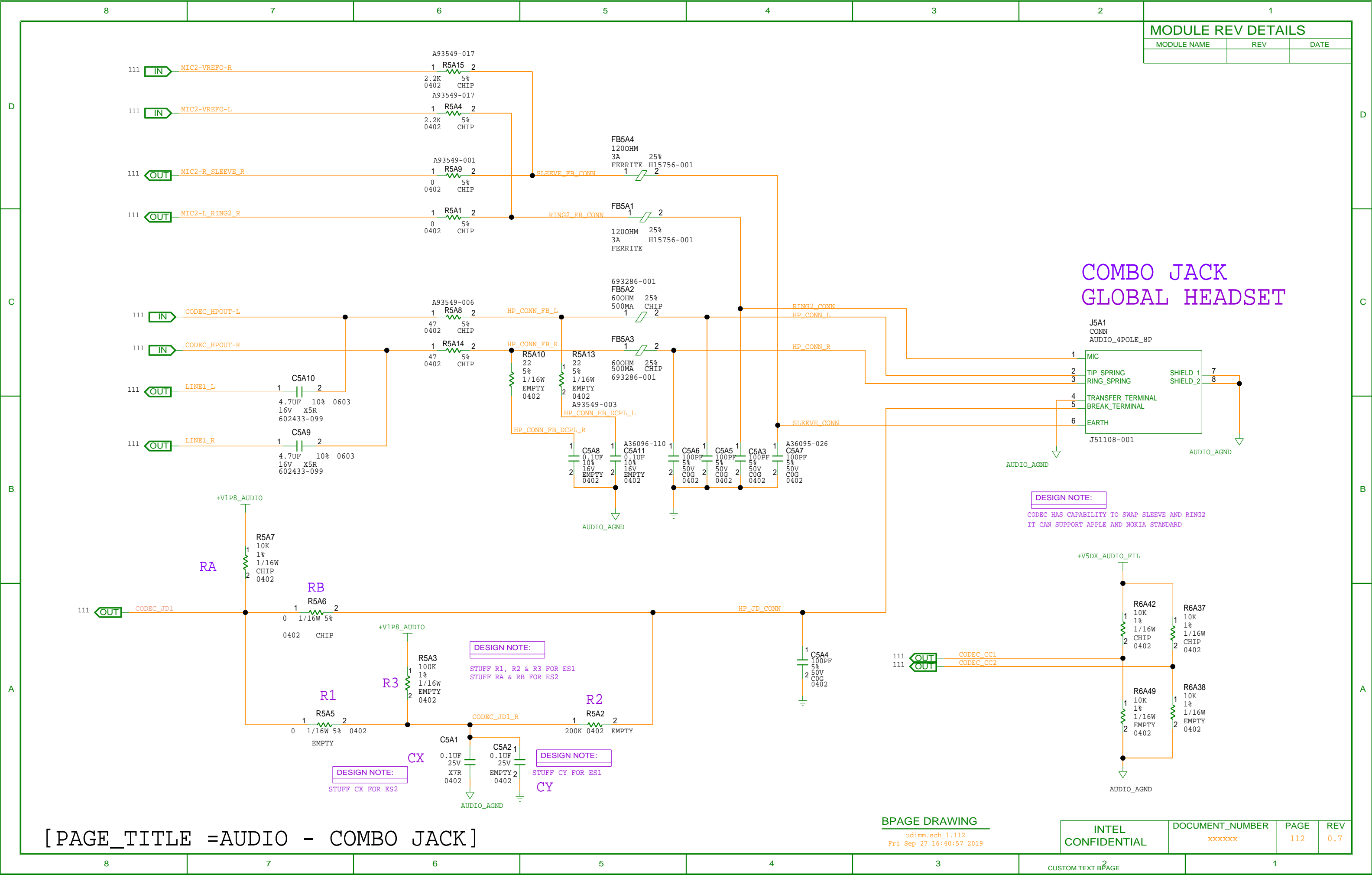


I2S\_MCLK LEVEL SHIFTER







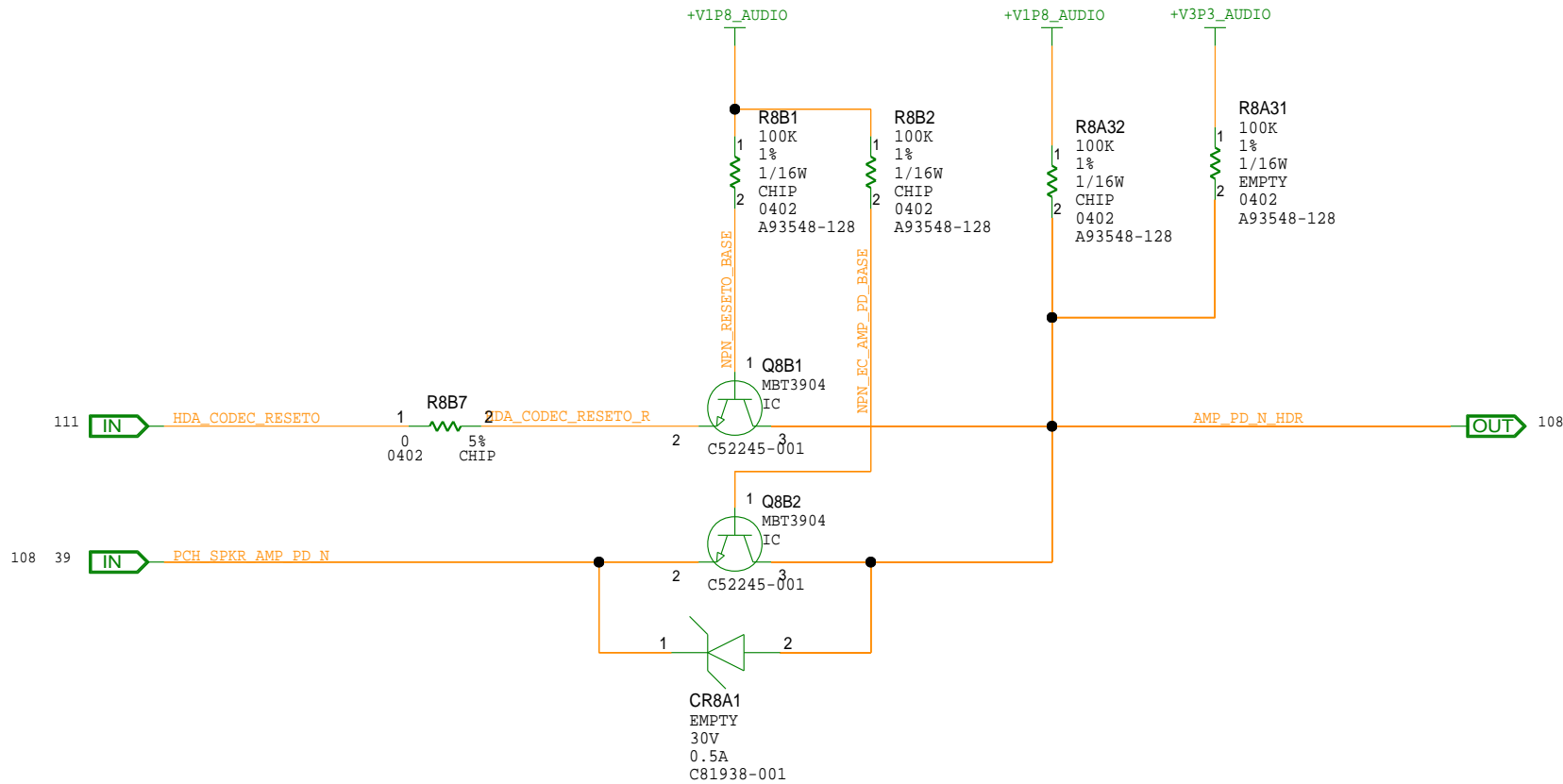




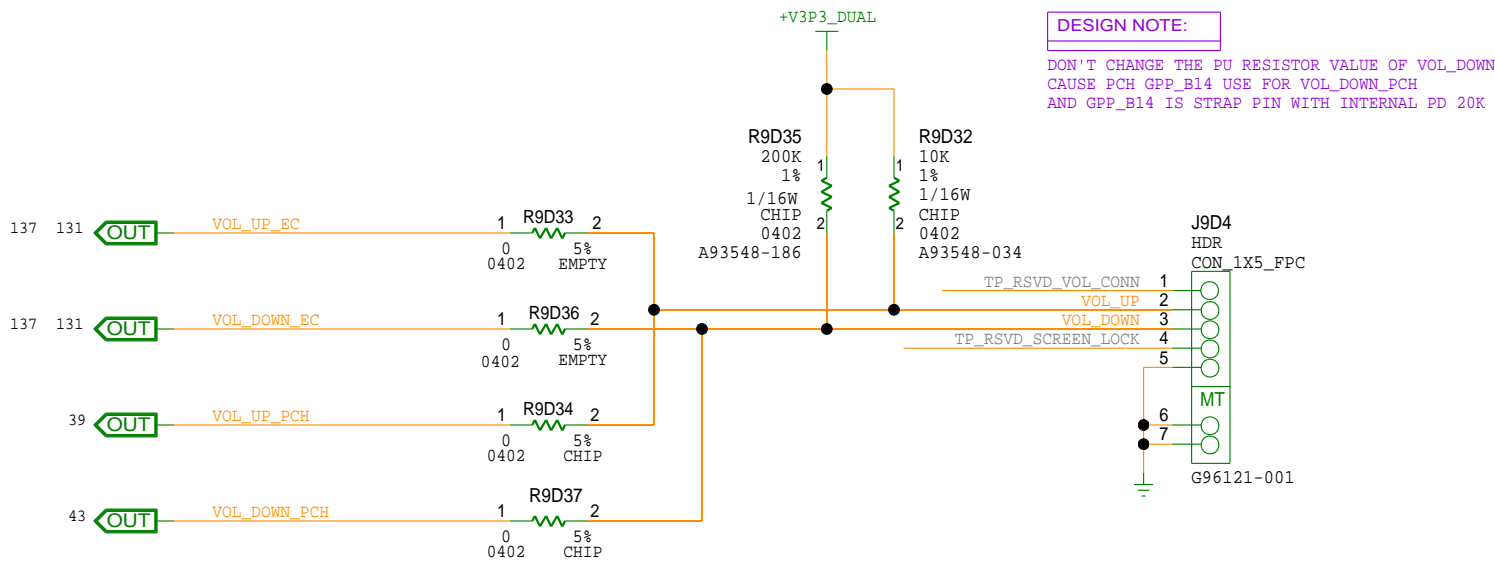
AMP POWER DOWN CIRCUIT

MODULE REV DETAILS

MODULE NAME	REV	DATE



VOLUME UP-DOWN HEADER



DESIGN NOTE:

DON'T CHANGE THE PU RESISTOR VALUE OF VOL\_DOWN  
CAUSE PCH GPP\_B14 USE FOR VOL\_DOWN\_PCH  
AND GPP\_B14 IS STRAP PIN WITH INTERNAL PD 20K

[PAGE\_TITLE =AUDIO -AMP PD, VOL CONTROL]

BPAGE DRAWING

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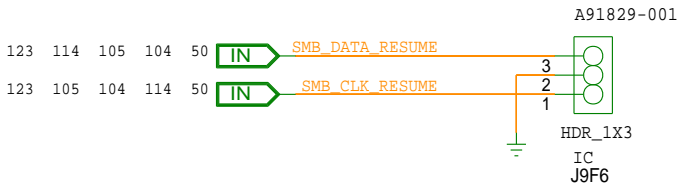
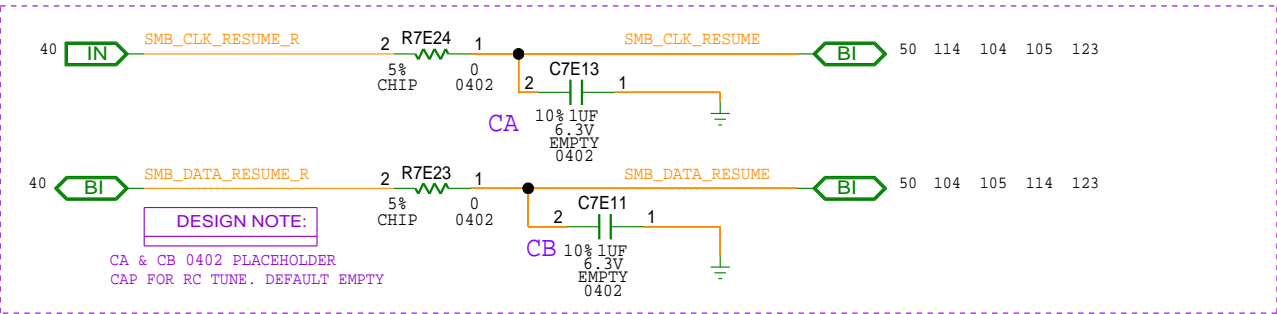
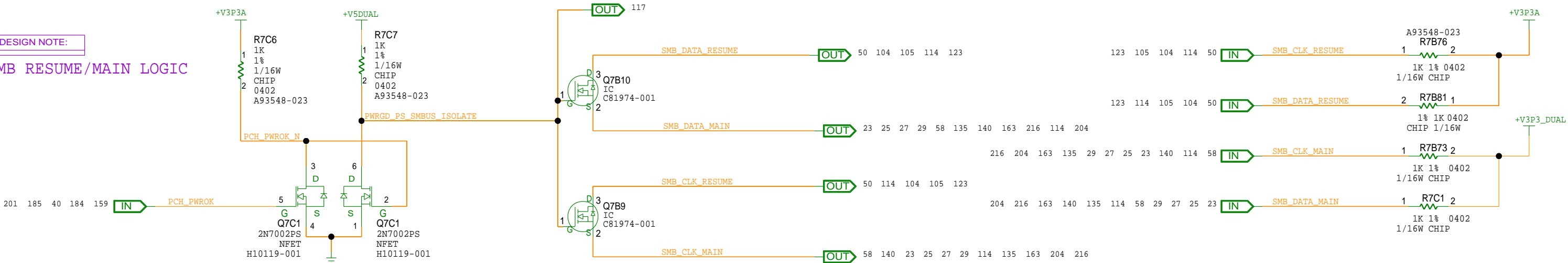
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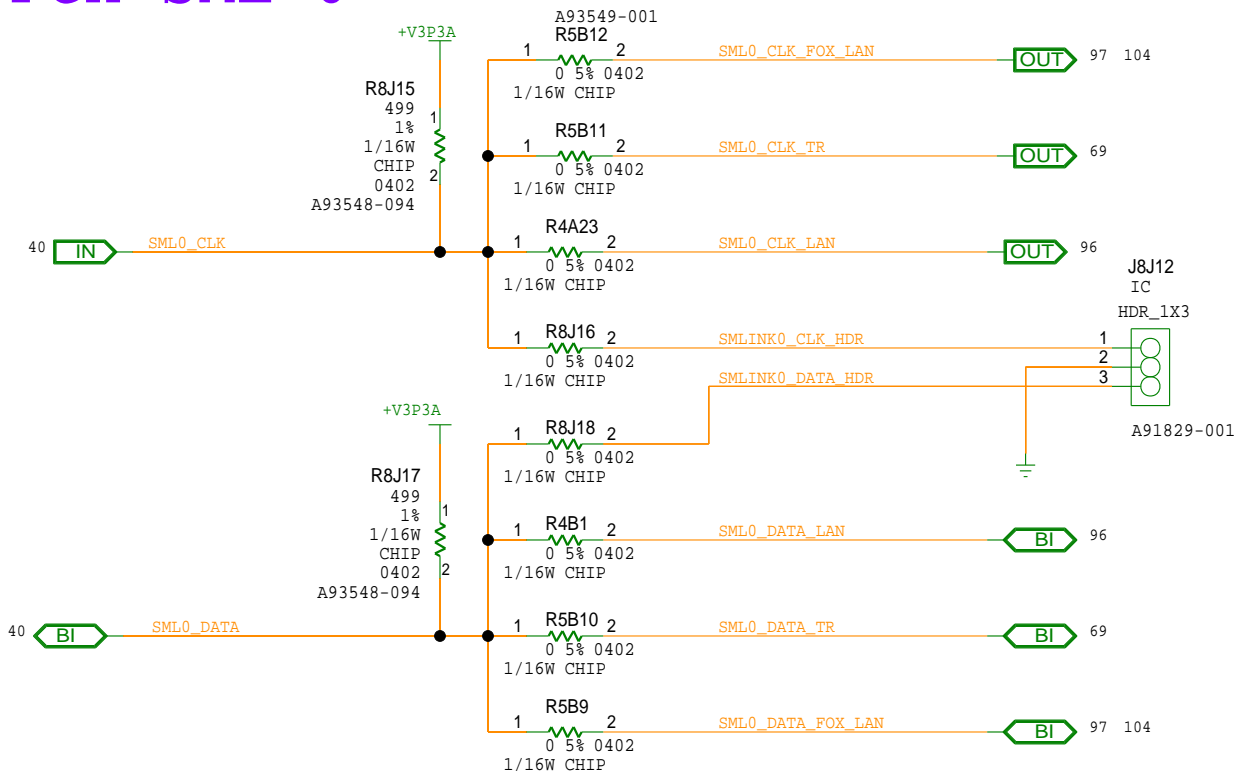


PCH SMBUS

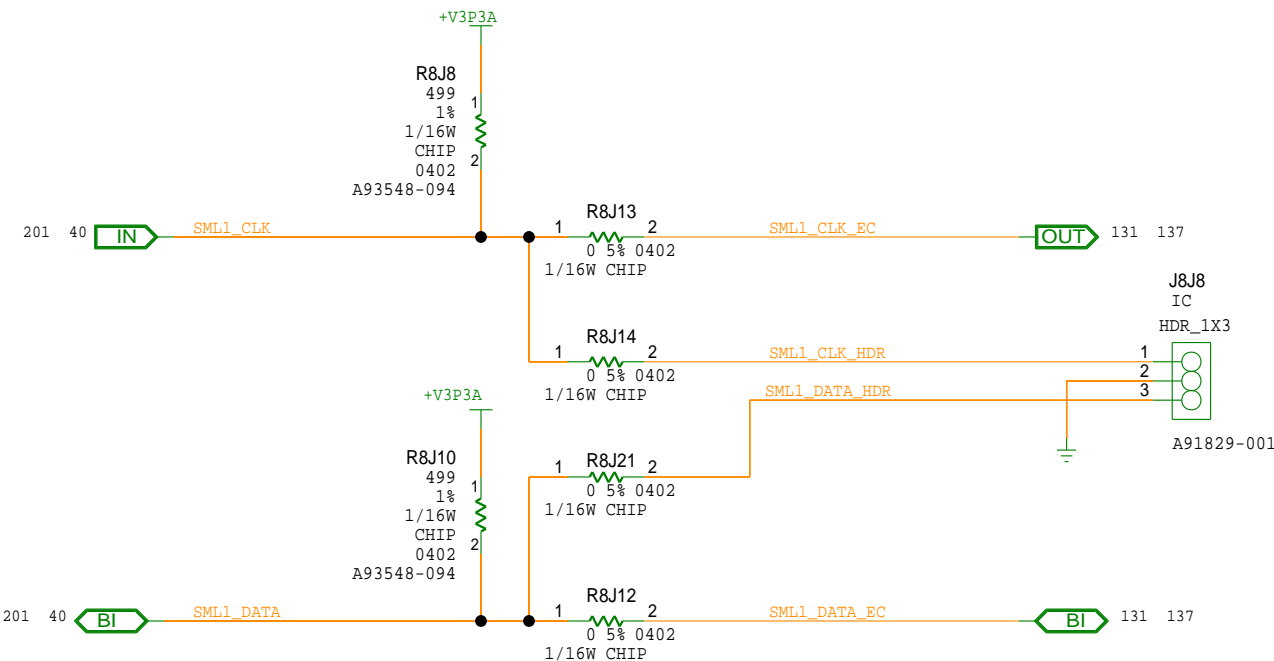
DESIGN NOTE:  
SMB RESUME/MAIN LOGIC



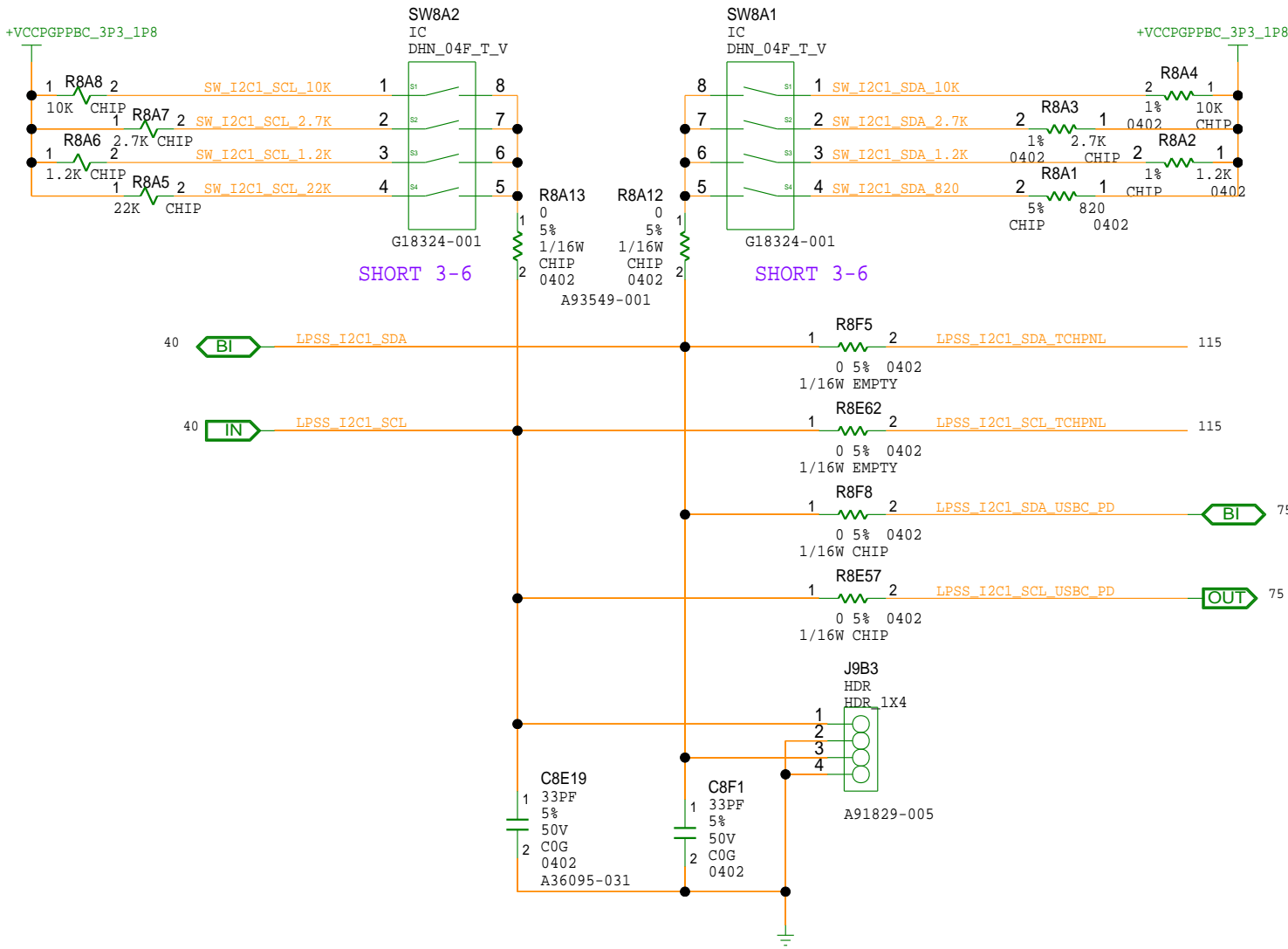
PCH SML 0



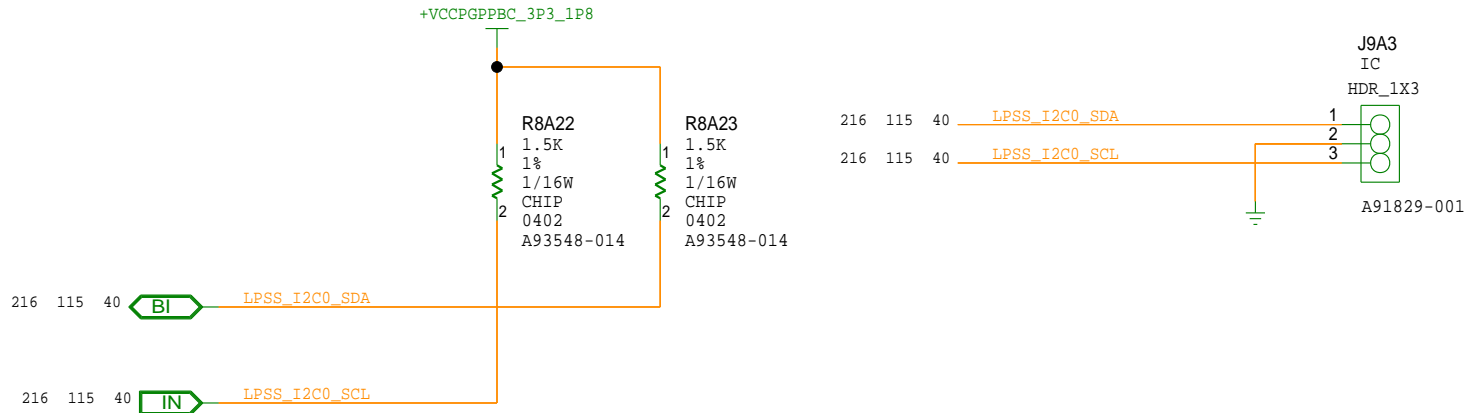
PCH SML 1



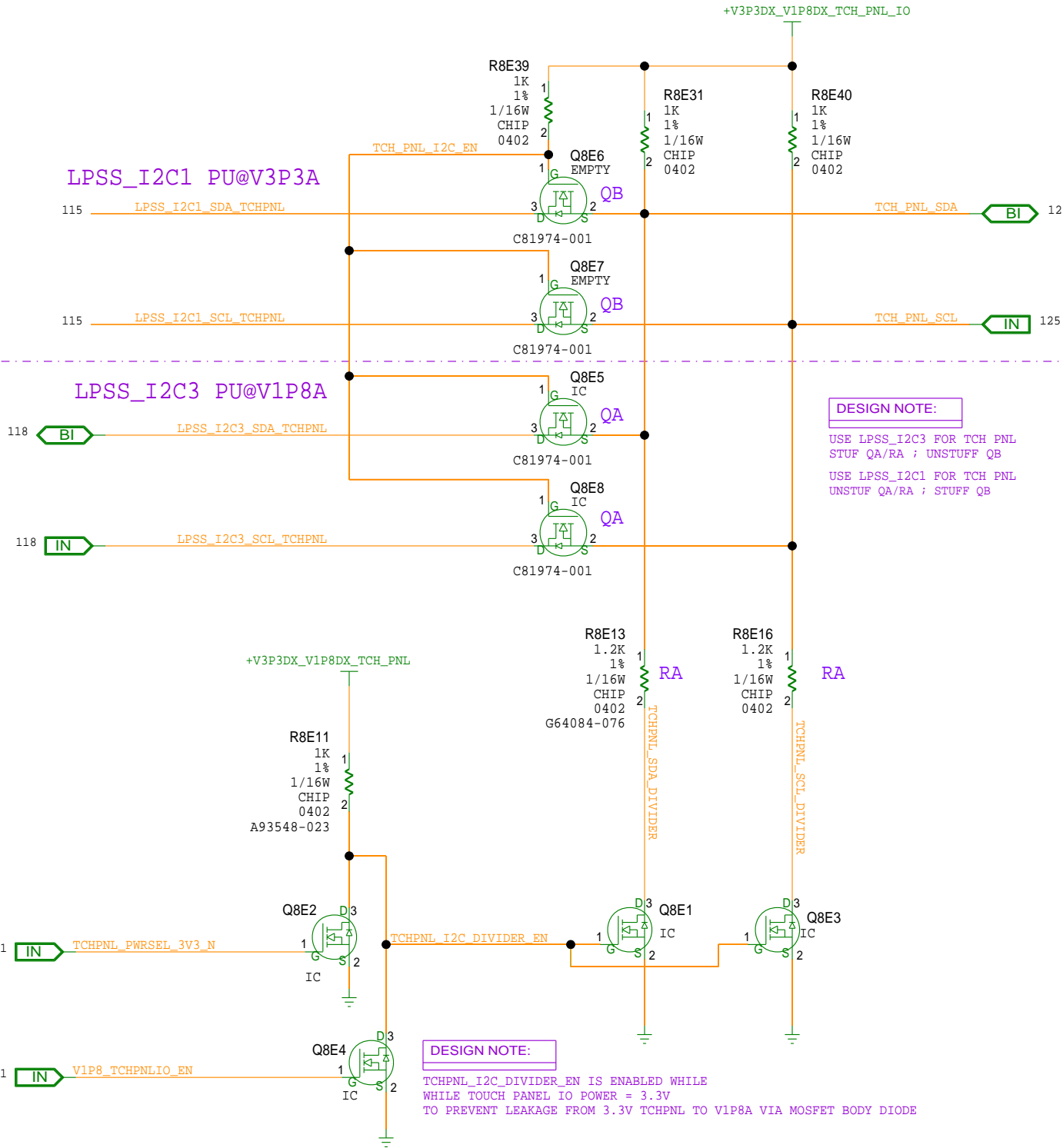
PCH LPSS I2C1



PCH LPSS I2C0



TOUCH PANEL I2C OPTIONS



DESIGN NOTE:  
USE LPSS\_I2C3 FOR TCH PNL  
STUF QA/RA ; UNSTUFF QB  
USE LPSS\_I2C1 FOR TCH PNL  
UNSTUF QA/RA ; STUFF QB

DESIGN NOTE:  
TCHPNL\_I2C\_DIVIDER\_EN IS ENABLED WHILE  
WHILE TOUCH PANEL IO POWER = 3.3V  
TO PREVENT LEAKAGE FROM 3.3V TCHPNL TO VIP8A VIA MOSFET BODY DIODE

LPSS - GSPI0/1 UART0/1 HEADER

MODULE REV DETAILS

MODULE NAME	REV	DATE

GSPI0

DESIGN NOTE:

00HM FOR 1.8V  
330HM FOR 3.3V

CAD NOTE:

PLACE R1 CLOSE TO PCH  
LPSS\_GSPI0\_MISO\_R

DESIGN NOTE:

R2 IS FOR DEBUG PURPOSE.  
NO SERIES RESISTOR REQUIRED

DESIGN NOTE:

00HM FOR 1.8V  
330HM FOR 3.3V

CAD NOTE:

PLACE R1 CLOSE TO PCH  
LPSS\_GSPI1\_MISO\_R

DESIGN NOTE:

R2 IS FOR DEBUG PURPOSE.  
NO SERIES RESISTOR REQUIRED

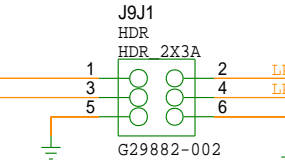
CAD NOTE:

PLACE THE HEADER IN EV AREA

UART0

UART0 PULL UP

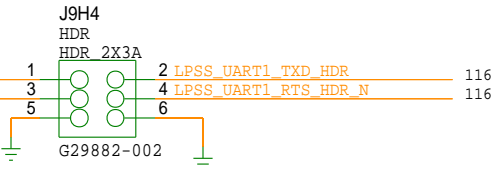
UART0 HEADER



LPSS/ISH UART1 SELECTION

LPSS UART1 HEADER

UART1 PULL UP



BPAGE DRAWING

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## D



## D



## B



BPAGE DRAWING

ISH I2C1 PU@SENSOR HEADER SIDE



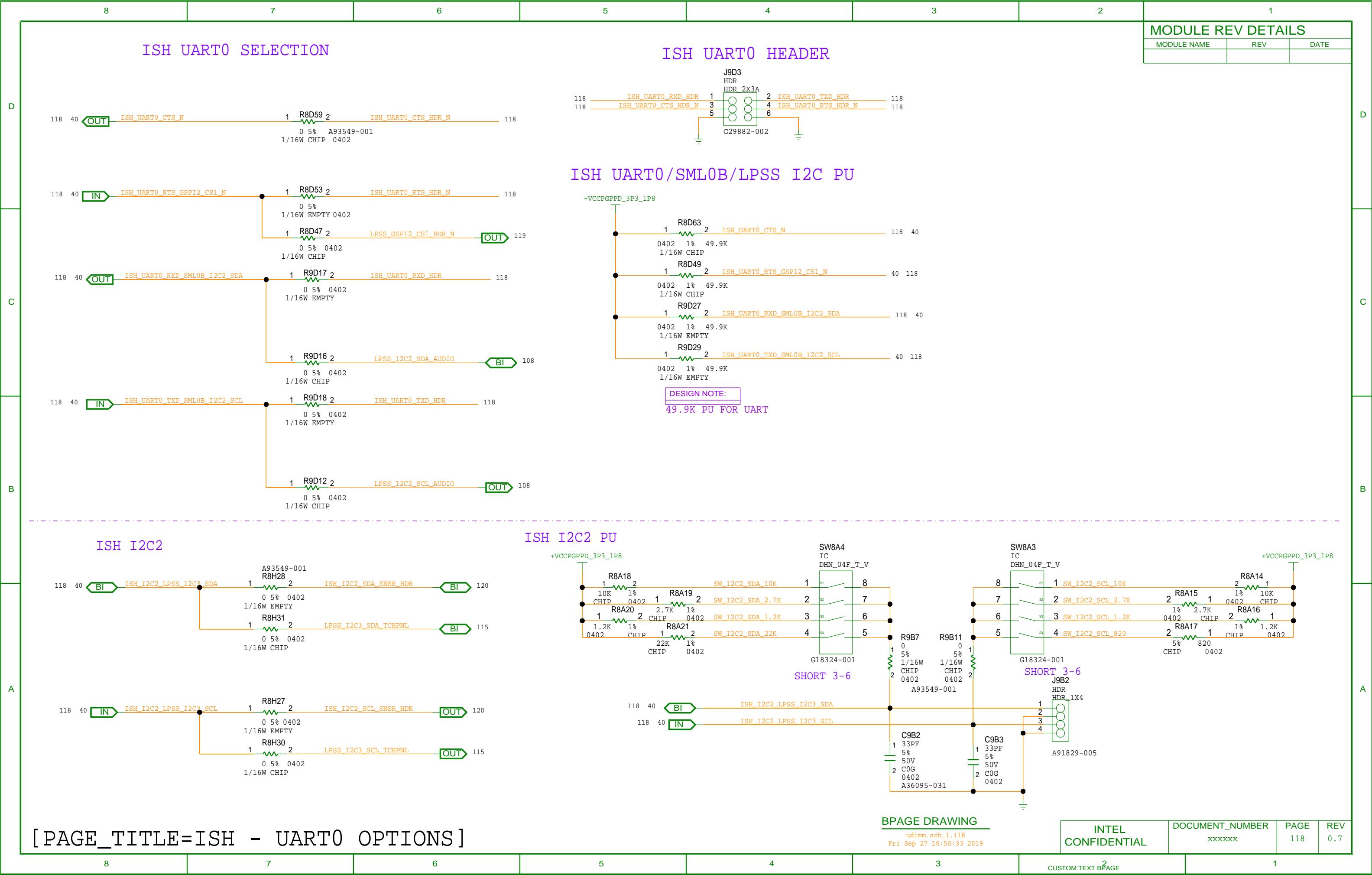
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117	0.7
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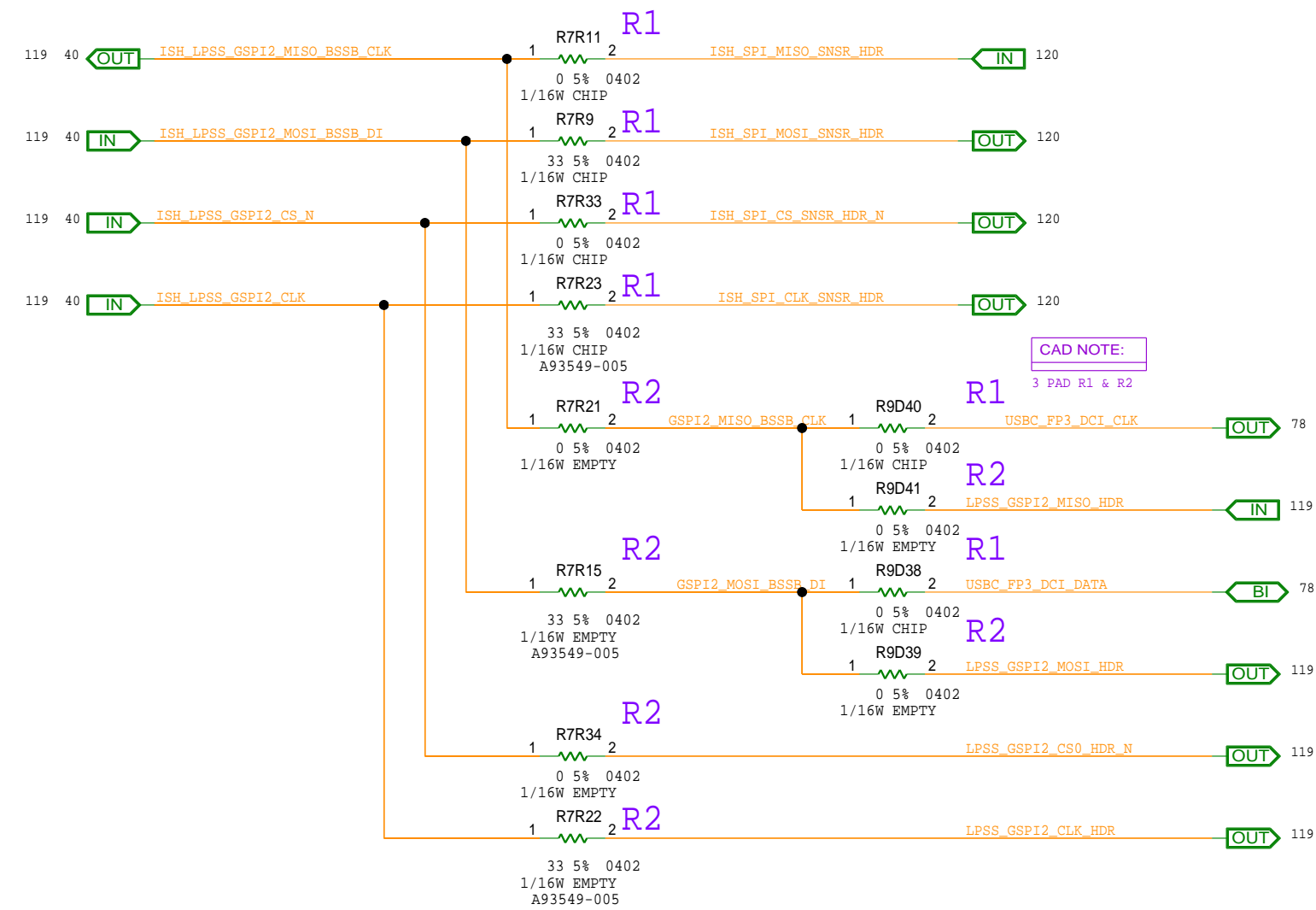


MODULE REV DETAILS

MODULE NAME	REV	DATE

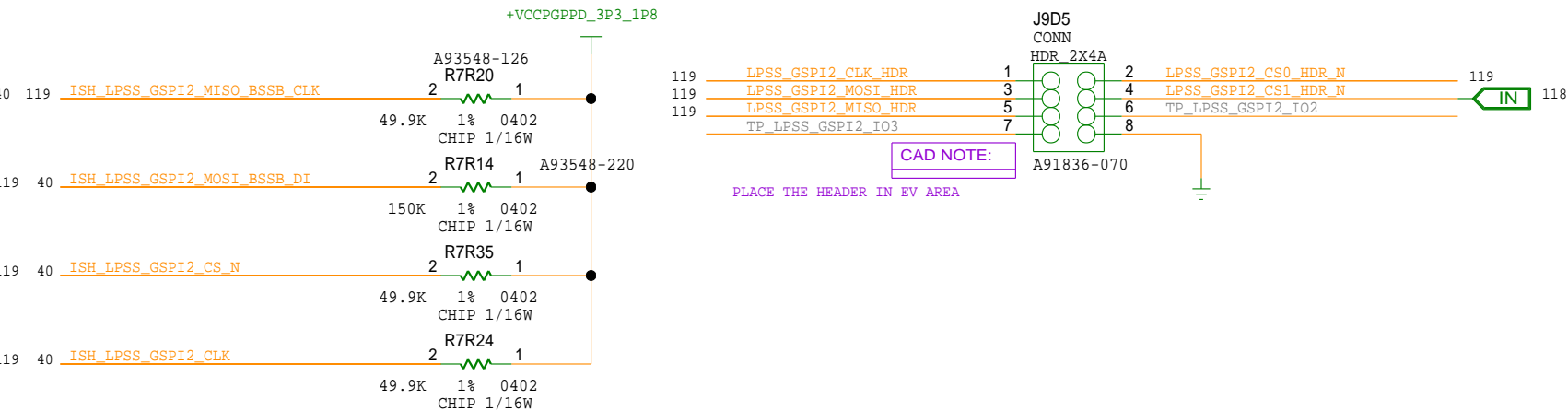
# ISH - ISH\_SPI / GPIO OPTIONS

## ISH SPI/LPSS GSPI2 SELECTION

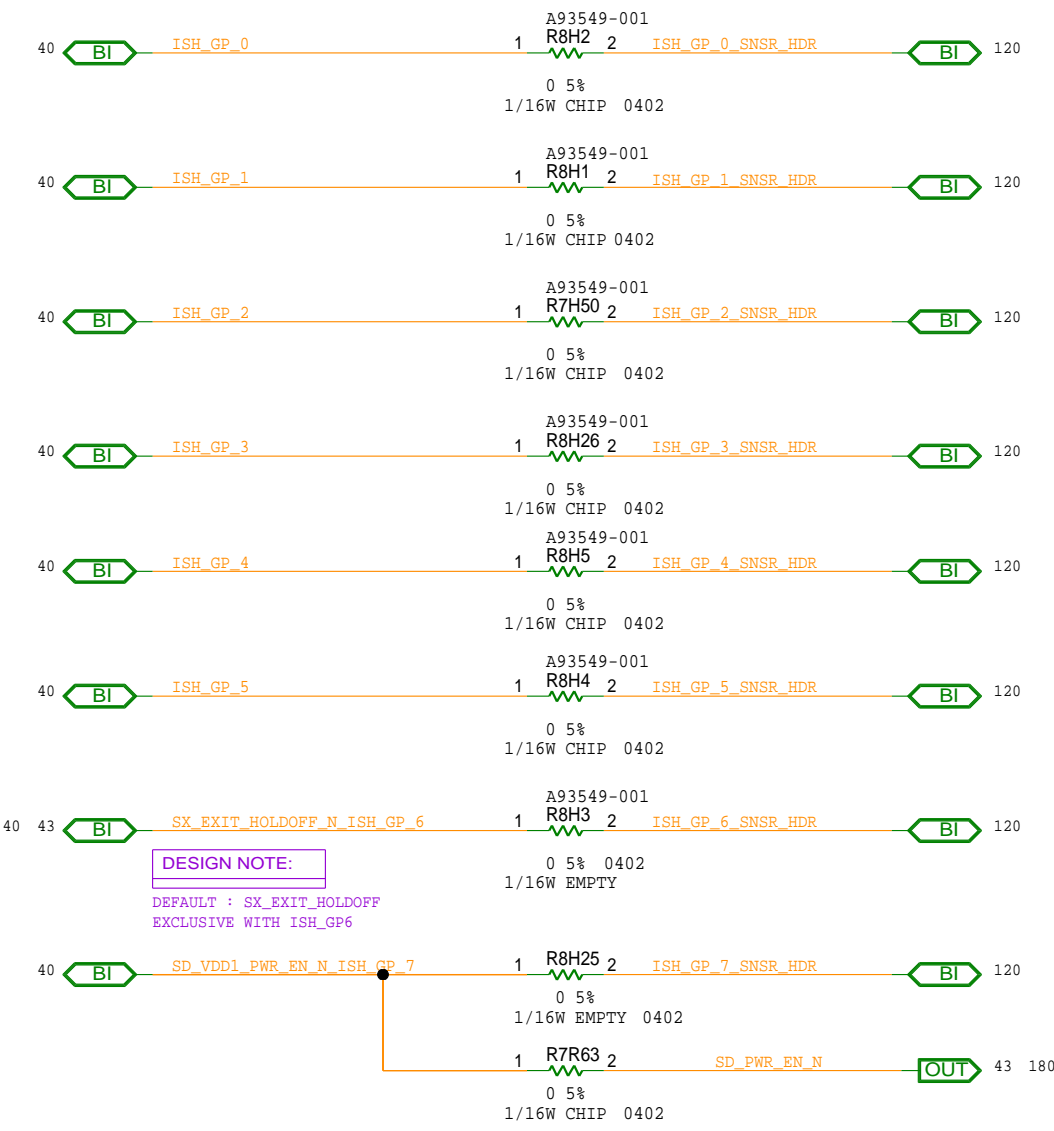


## ISH LPSS GSPI PULL-UP

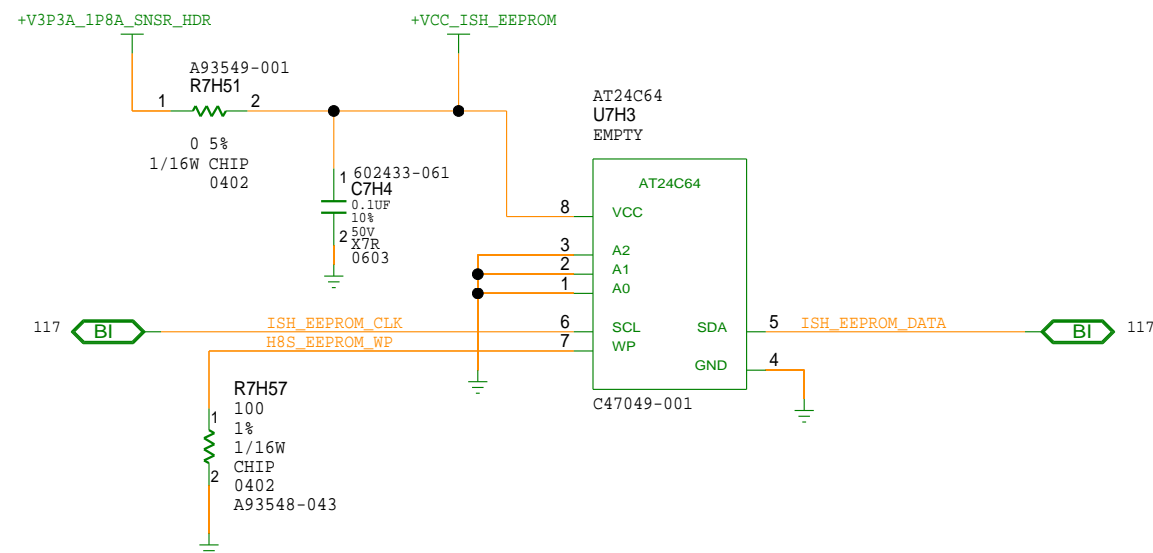
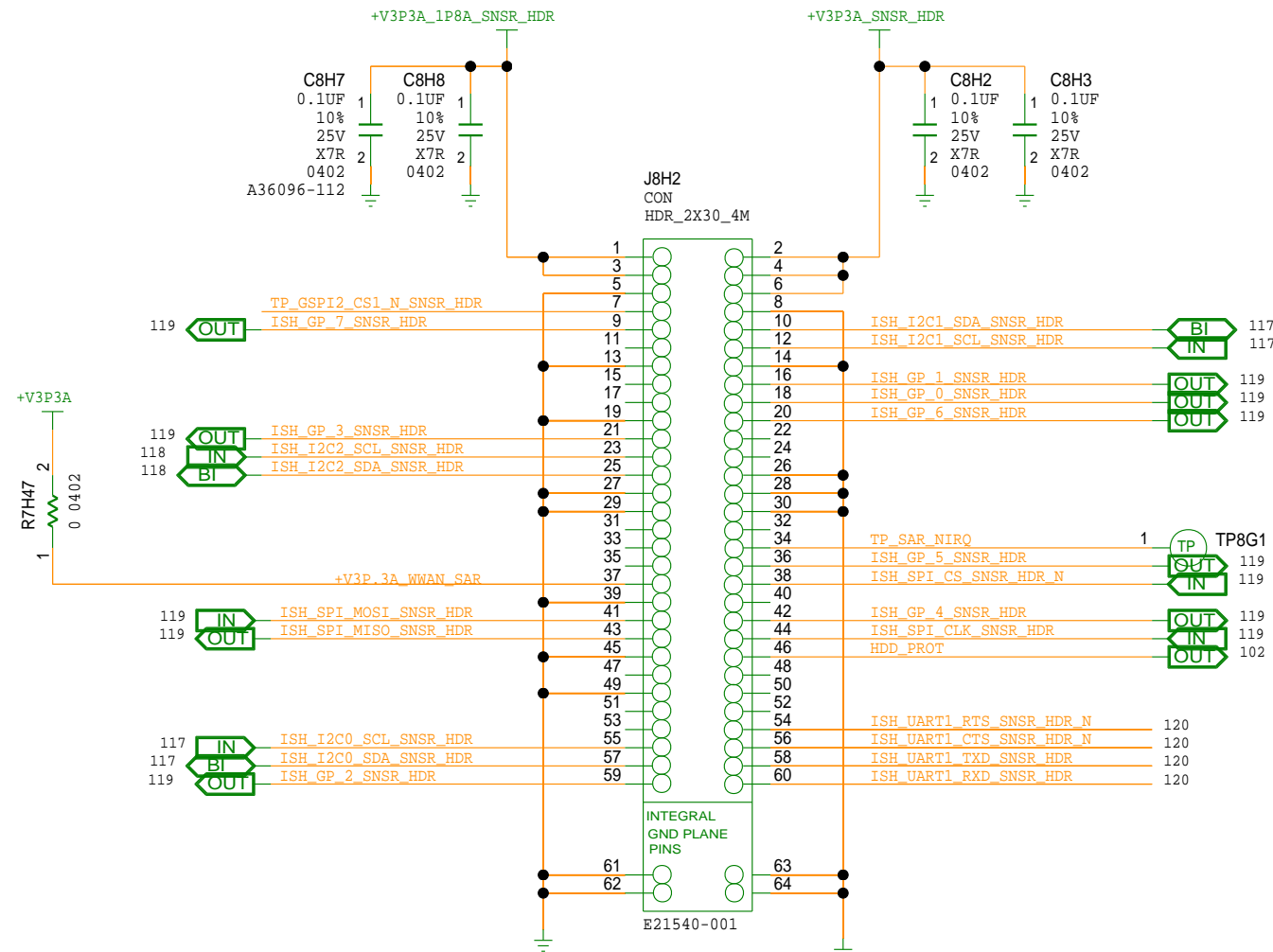
## GSPI2 HEADER



## ISH GPP SELECTION







The diagram illustrates the pin configuration and signal connections for the SN74AVC4T774 IC, which is a 16-pin device. The IC is labeled E57797-001.

**Pin Connections:**

- V1P8A:** Connected to pin 16 (VCCA).
- VCCP:** Connected to pin 15 (VCCB).
- V1P8:** Connected to pin 17 (GND THPAD).
- UART1 Signals:**
  - Pin 3: A1, ISH\_UART1\_RXD\_SNSR\_HDR
  - Pin 4: A2, ISH\_UART1\_TXD\_SNSR\_HDR
  - Pin 5: A3, ISH\_UART1\_RTS\_SNSR\_HDR\_N
  - Pin 6: A4, ISH\_UART1\_CTS\_SNSR\_HDR\_N
  - Pin 7: DIR1, UART1\_DIR1
  - Pin 8: DIR2, UART1\_DIR2
  - Pin 9: DIR3, UART1\_DIR3
  - Pin 10: DIR4, UART1\_DIR4
  - Pin 11: OE\_N, UART1\_OE\_N

**Component Values:**

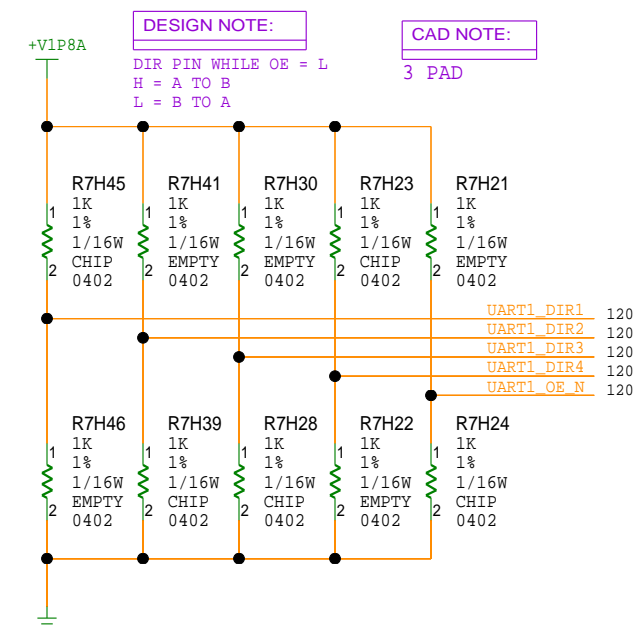
- C7H2:** 0.1UF, 10%, 25V, X7R, 0402, A36096-112
- C7H1:** 0.1UF, 10%, 25V, X7R, 0402, A36096-112

**IC Label:** SN74AVC4T774

**Part Number:** E57797-001

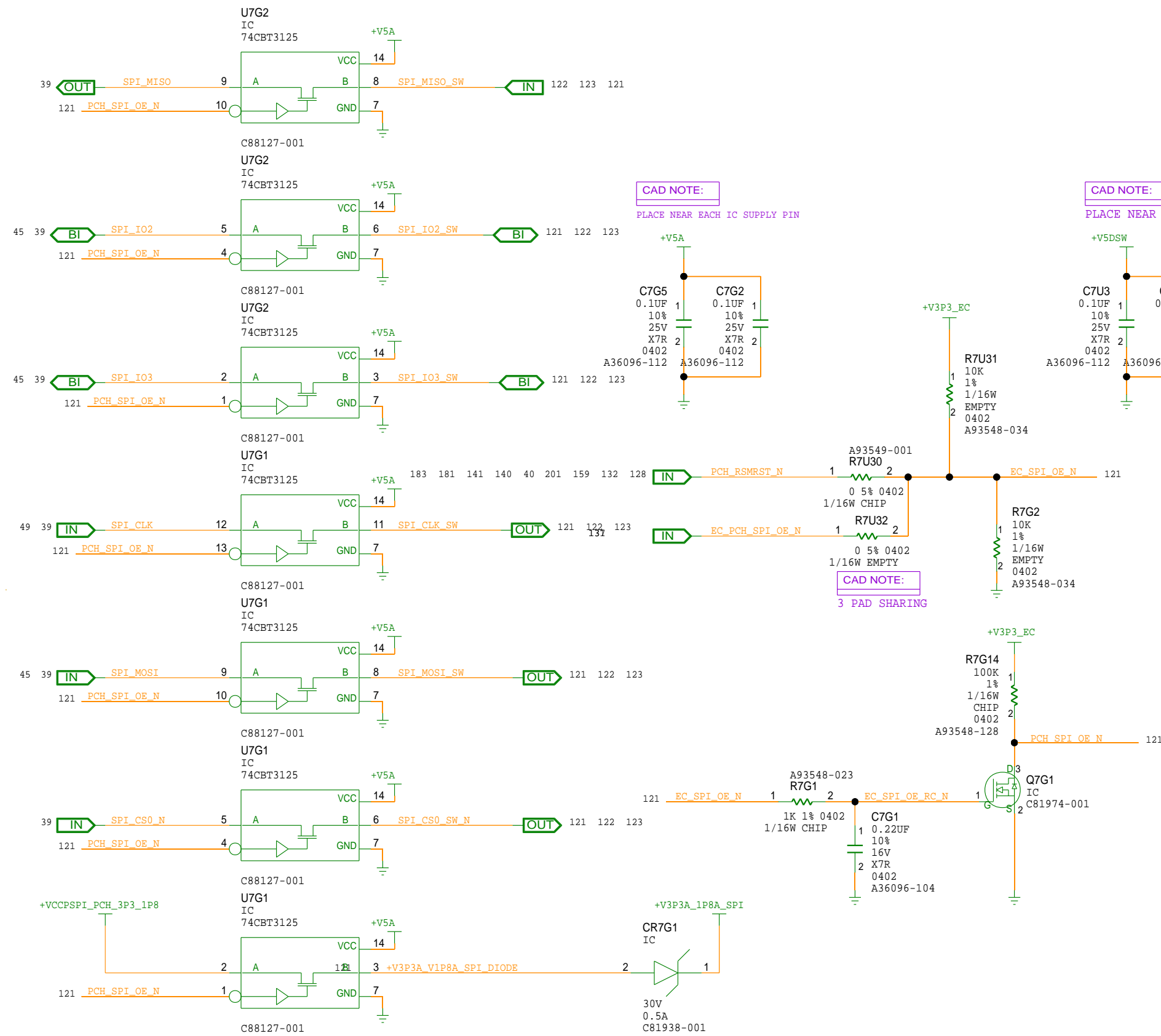
Timing diagram for ISH UART1 signals. The diagram shows four signal traces, each with a transition from 0 to 5% at 0402, followed by a 1/16W EMPTY period. The signals are connected to OUT and IN pins.

- ISH\_UART1\_RXD\_SNSR\_HDR (R7H40):** Signal transition from 0 to 5% at 0402, followed by 1/16W EMPTY. Connected to OUT pin.
- ISH\_UART1\_TXD\_SNSR\_HDR (R7H35):** Signal transition from 0 to 5% at 0402, followed by 1/16W EMPTY. Connected to IN pin.
- ISH\_UART1\_RTS\_SNSR\_HDR\_N (R7H31):** Signal transition from 0 to 5% at 0402, followed by 1/16W EMPTY. Connected to IN pin.
- ISH\_UART1\_CTS\_SNSR\_HDR\_N (R7H29):** Signal transition from 0 to 5% at 0402, followed by 1/16W EMPTY. Connected to OUT pin.

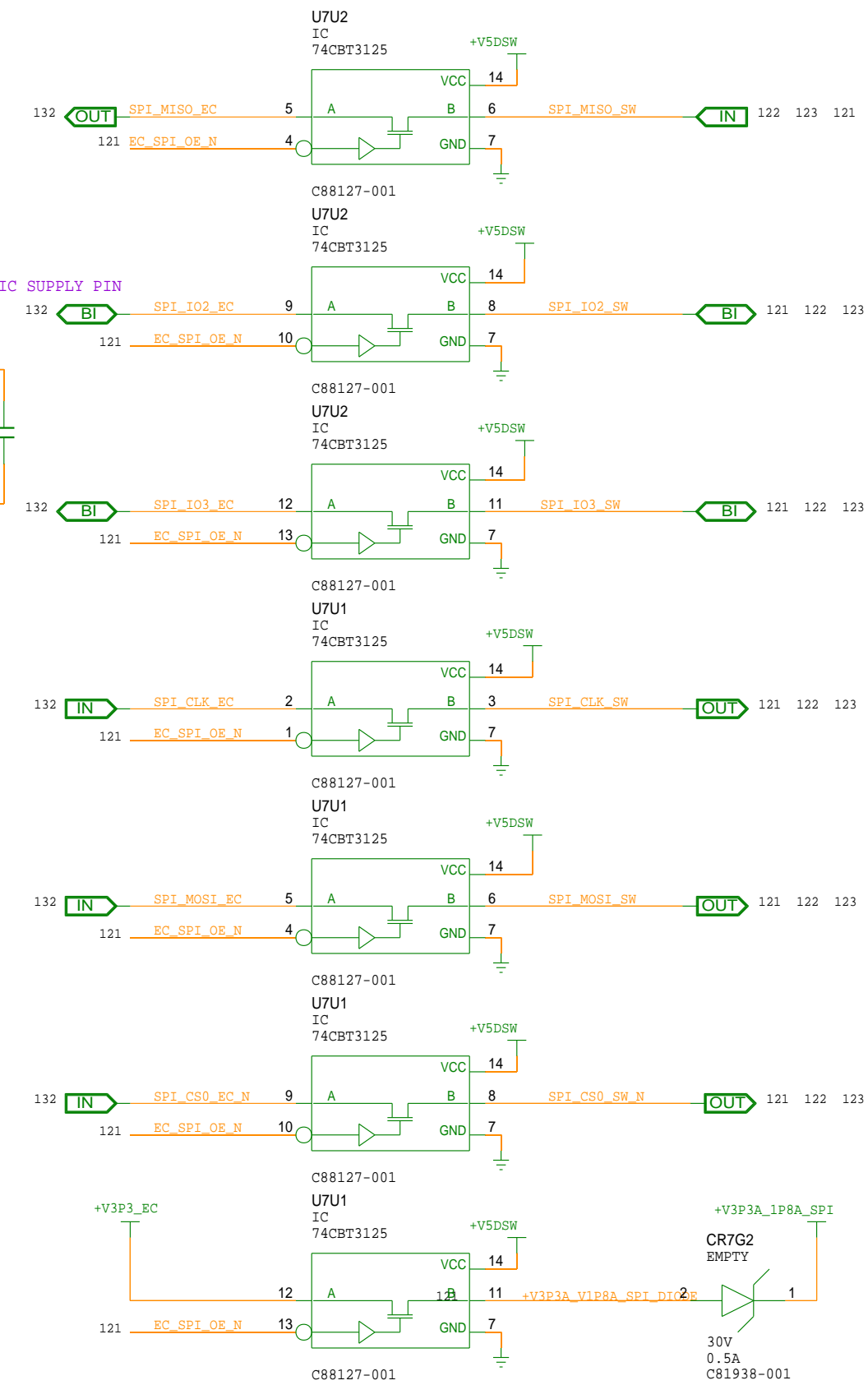


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PCH SPI G3 FLASH PROGRAMMING ISOLATION CIRCUIT



PCH-EC FLASH SHARING WITH WIRED-OR TOPOLOGY



MODULE REV DETAILS

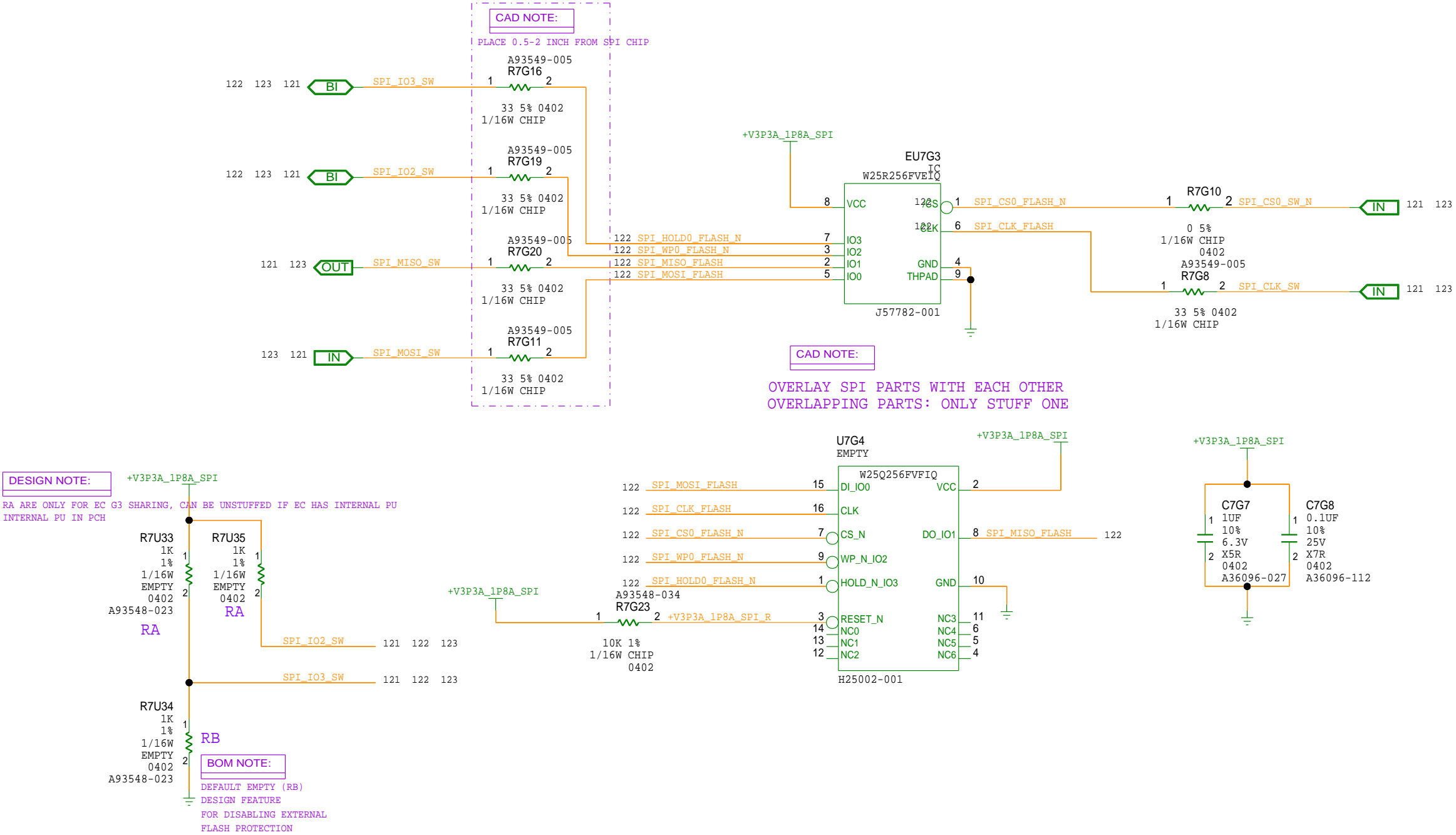
MODULE NAME	REV	DATE



MODULE REV DETAILS

MODULE NAME	REV	DATE

PRIMARY SERIAL FLASH



D

135	LPSS_UART2_RXD_TTK	IO7	IO8	8	EC_UART_RX_TTK	OUT	123	135
135	LPSS_UART2_TXD_TTK	IO9	IO10	12	EC_UART_TX_TTK	IN	135	123
	LPSS_UART2_CTS_TTK							
	LPSS_UART2_RTS_TTK							

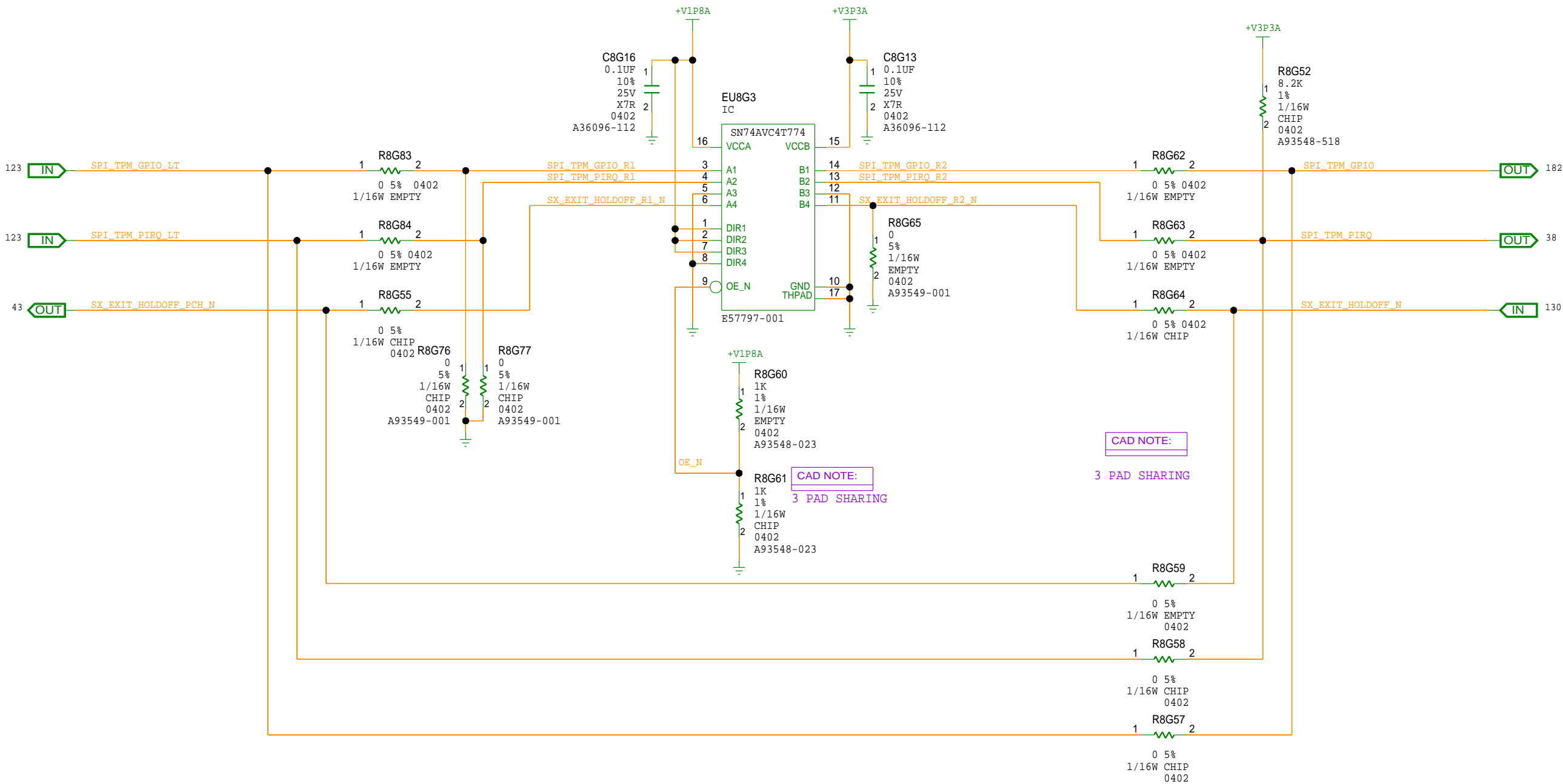


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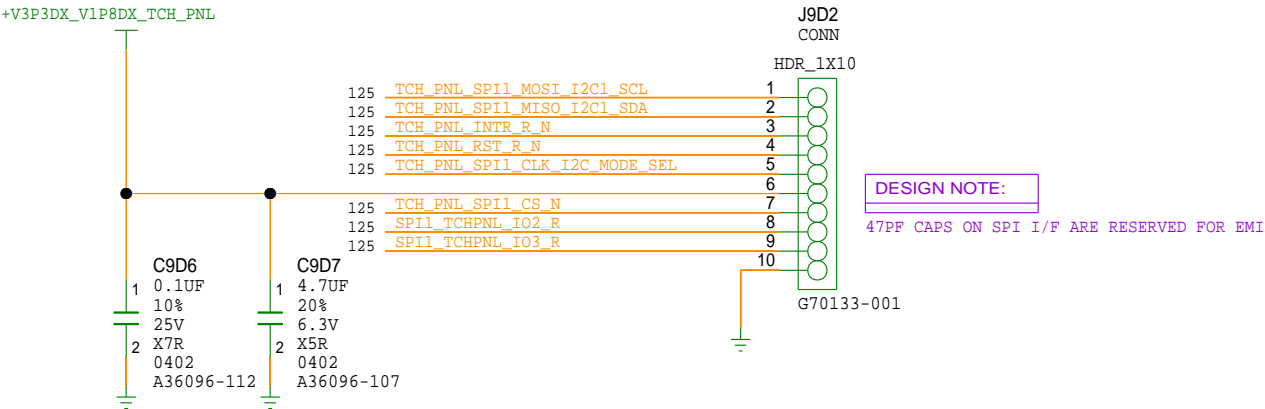
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MODULE REV DETAILS

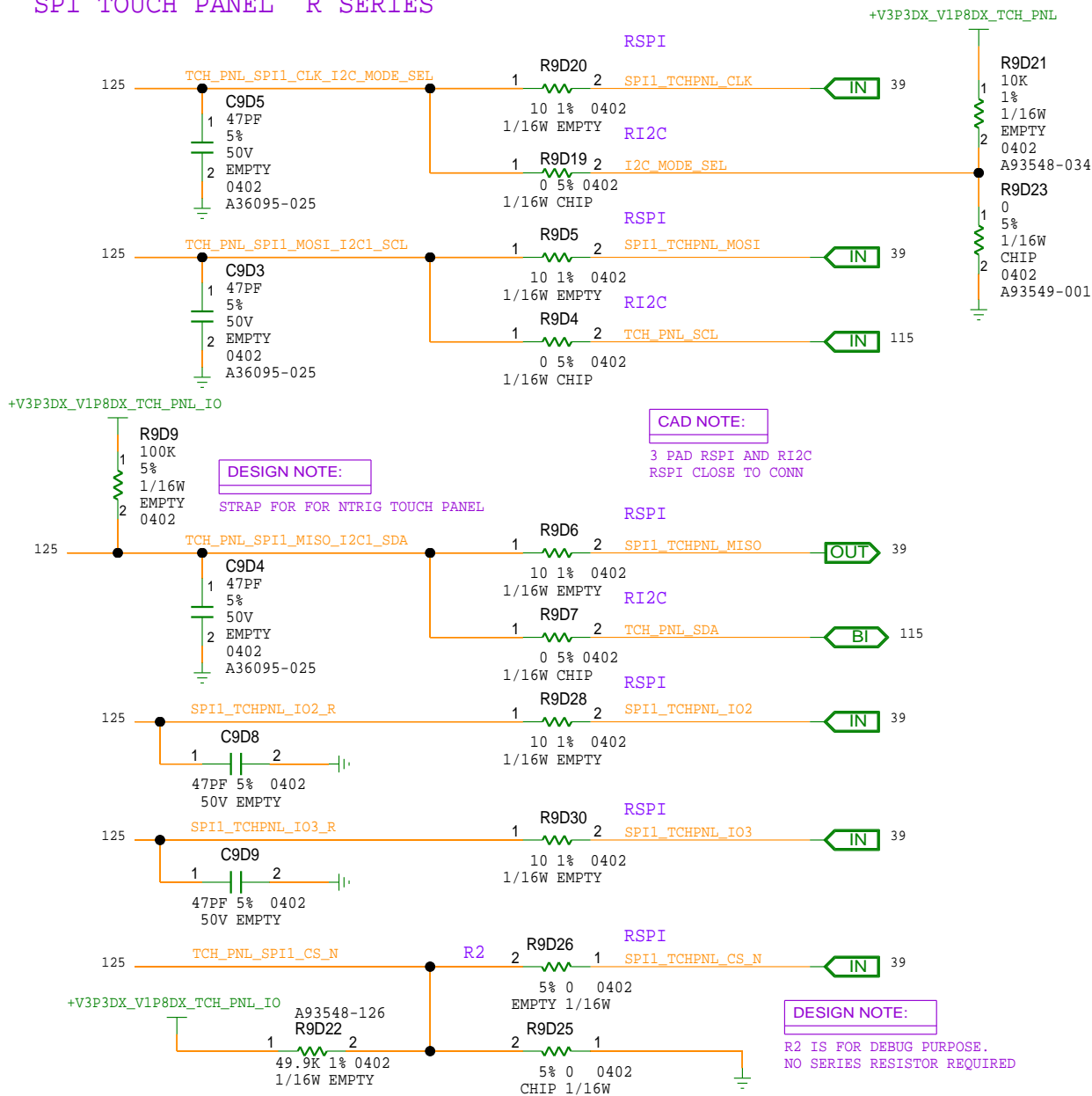
MODULE NAME	REV	DATE



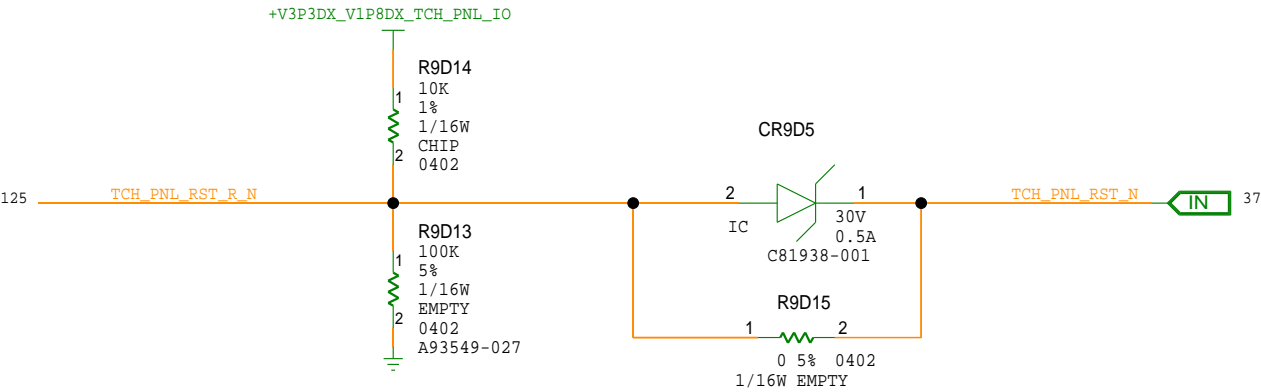
I2C/SPI TOUCH PANEL CONNECTOR



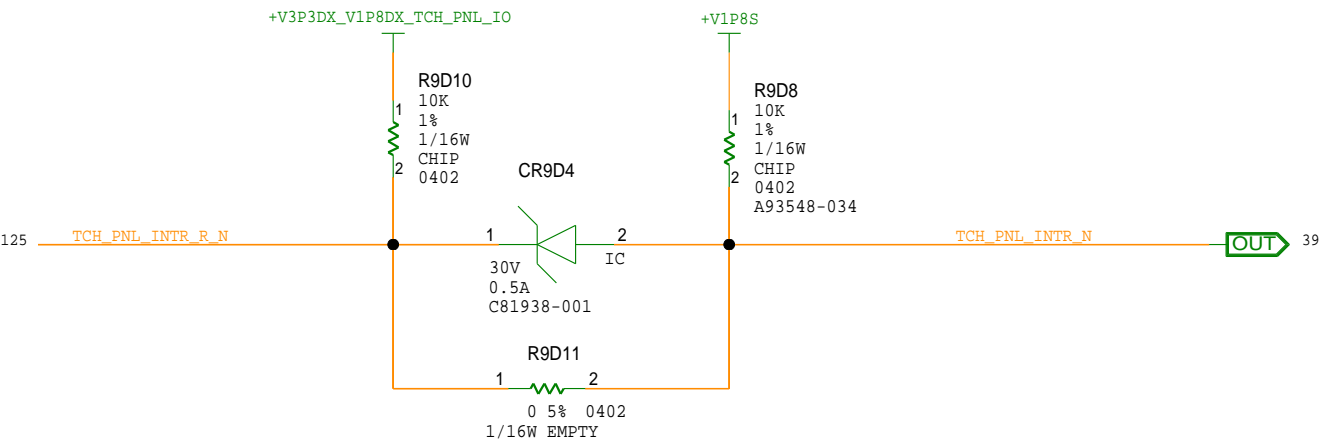
SPI TOUCH PANEL R SERIES



I2C TOUCH PANEL RST

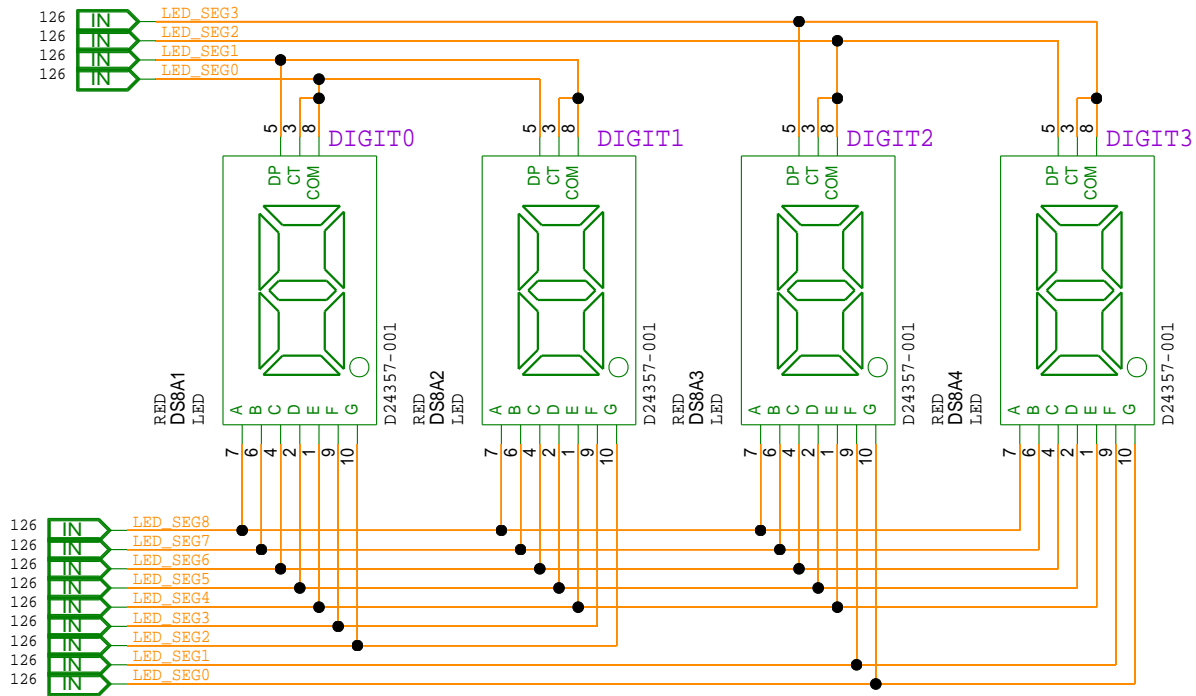
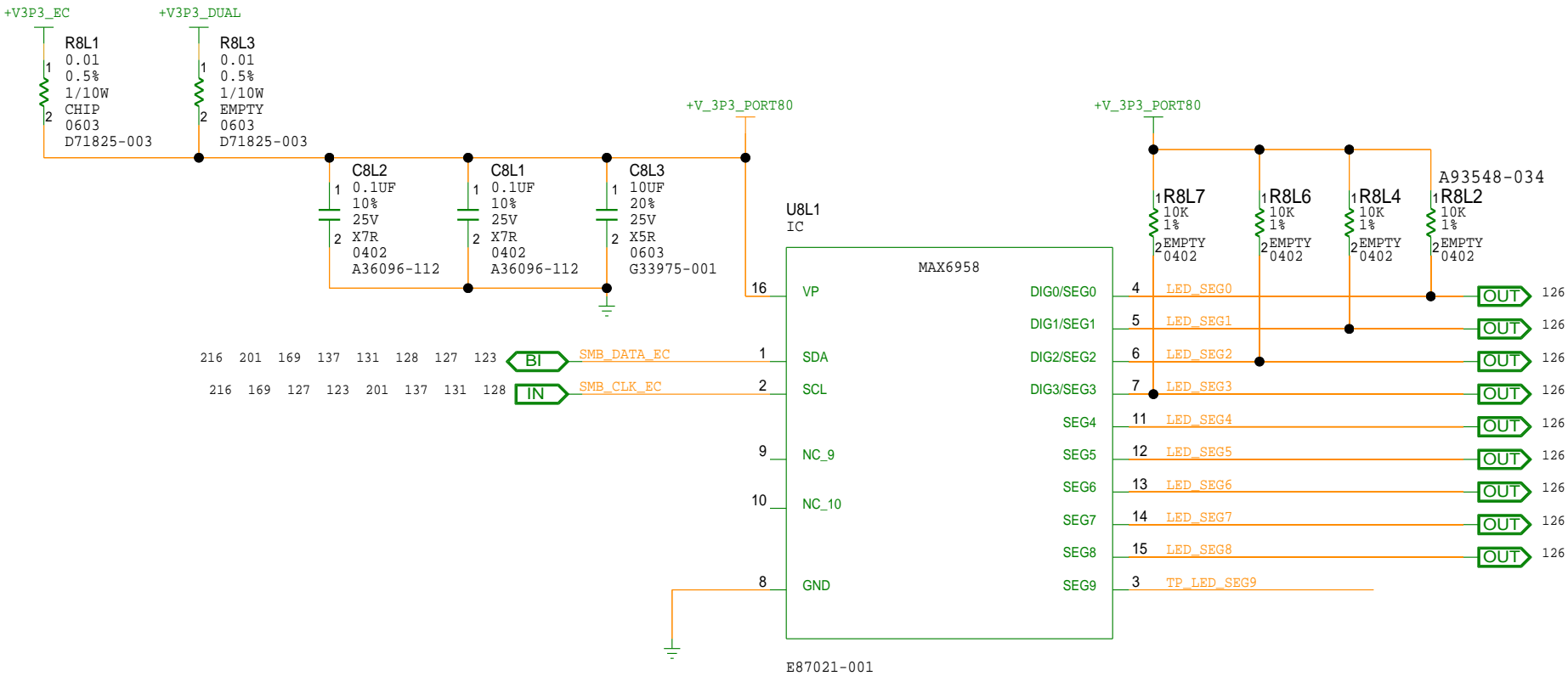


I2C TOUCH PANEL INTERRUPT

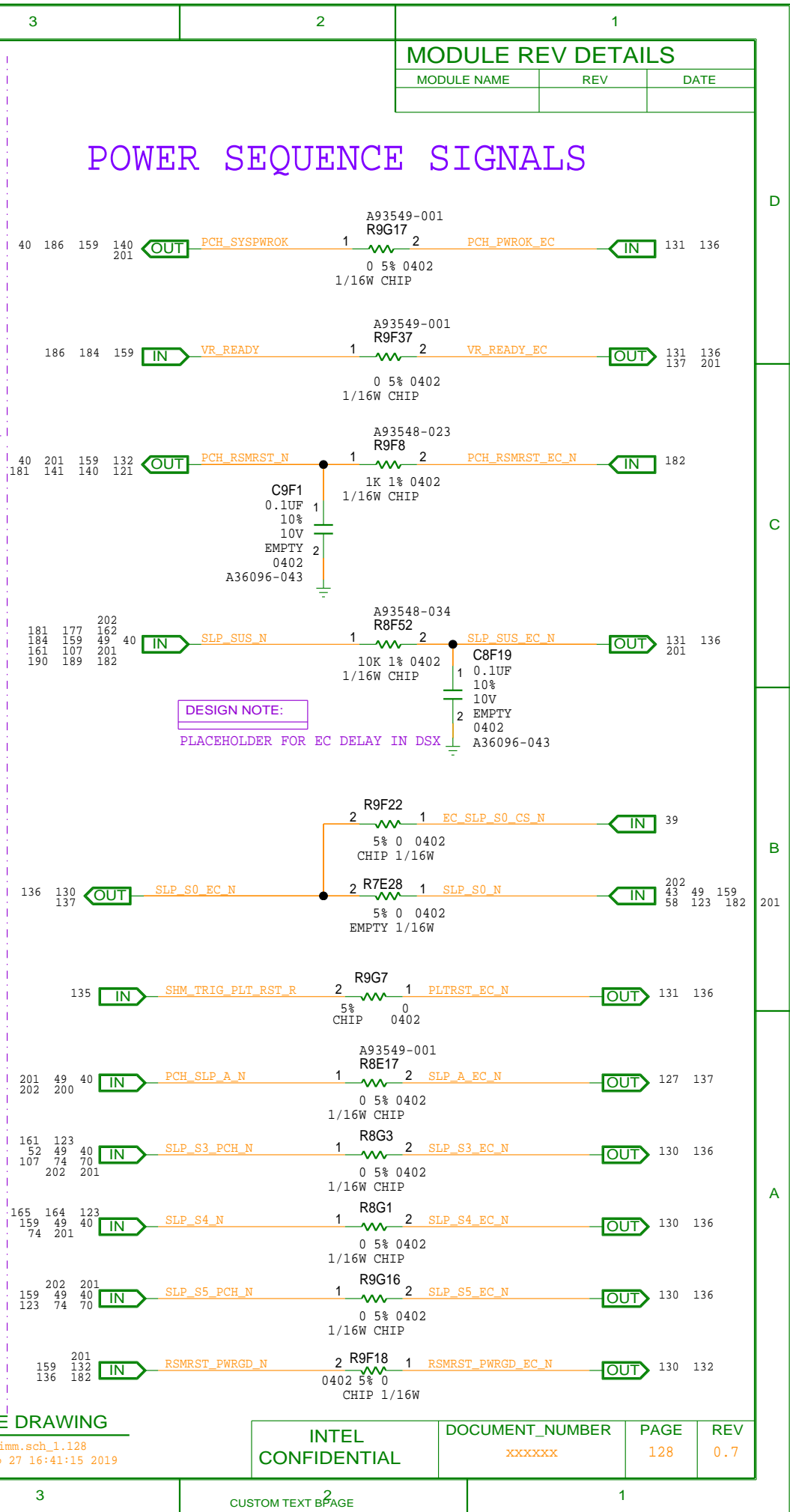
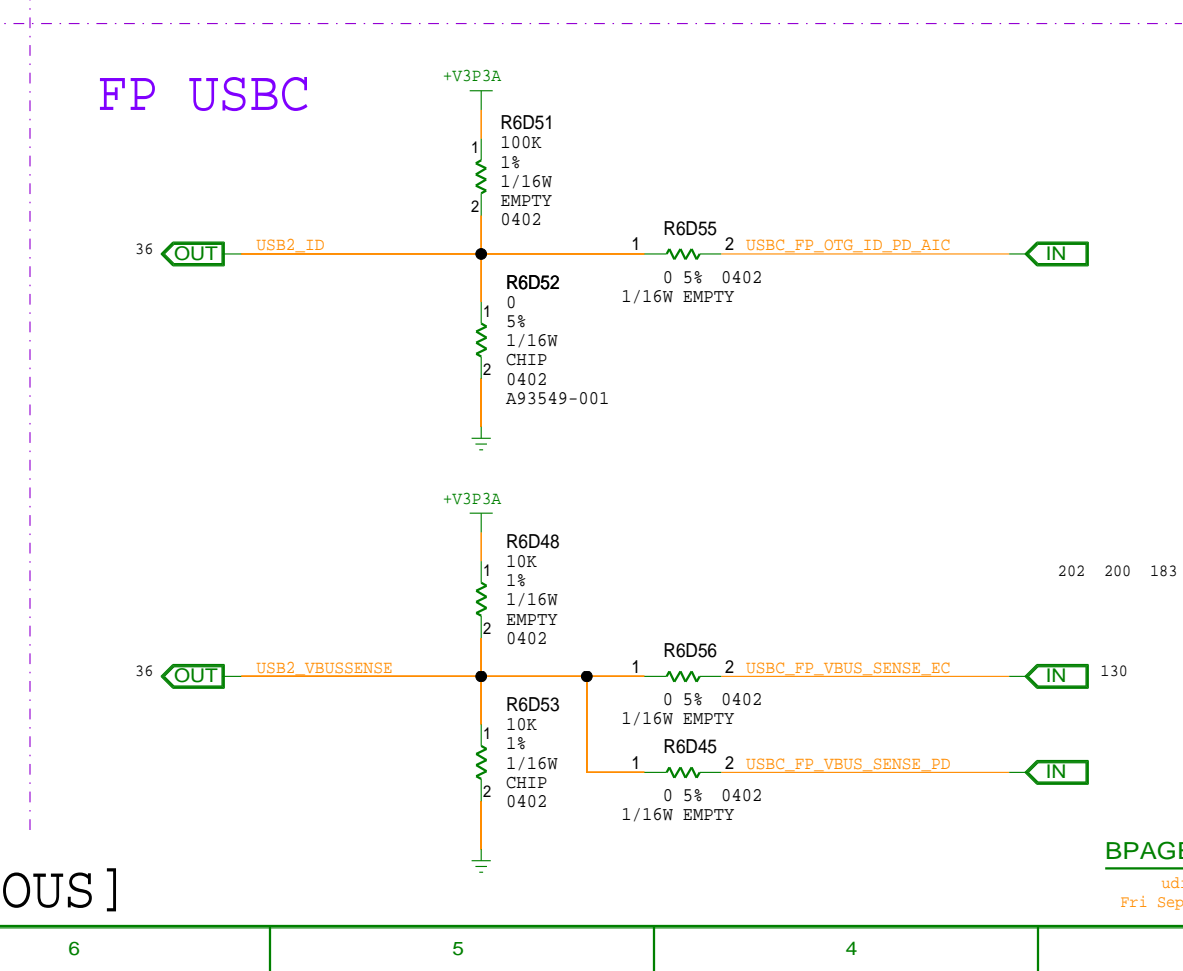
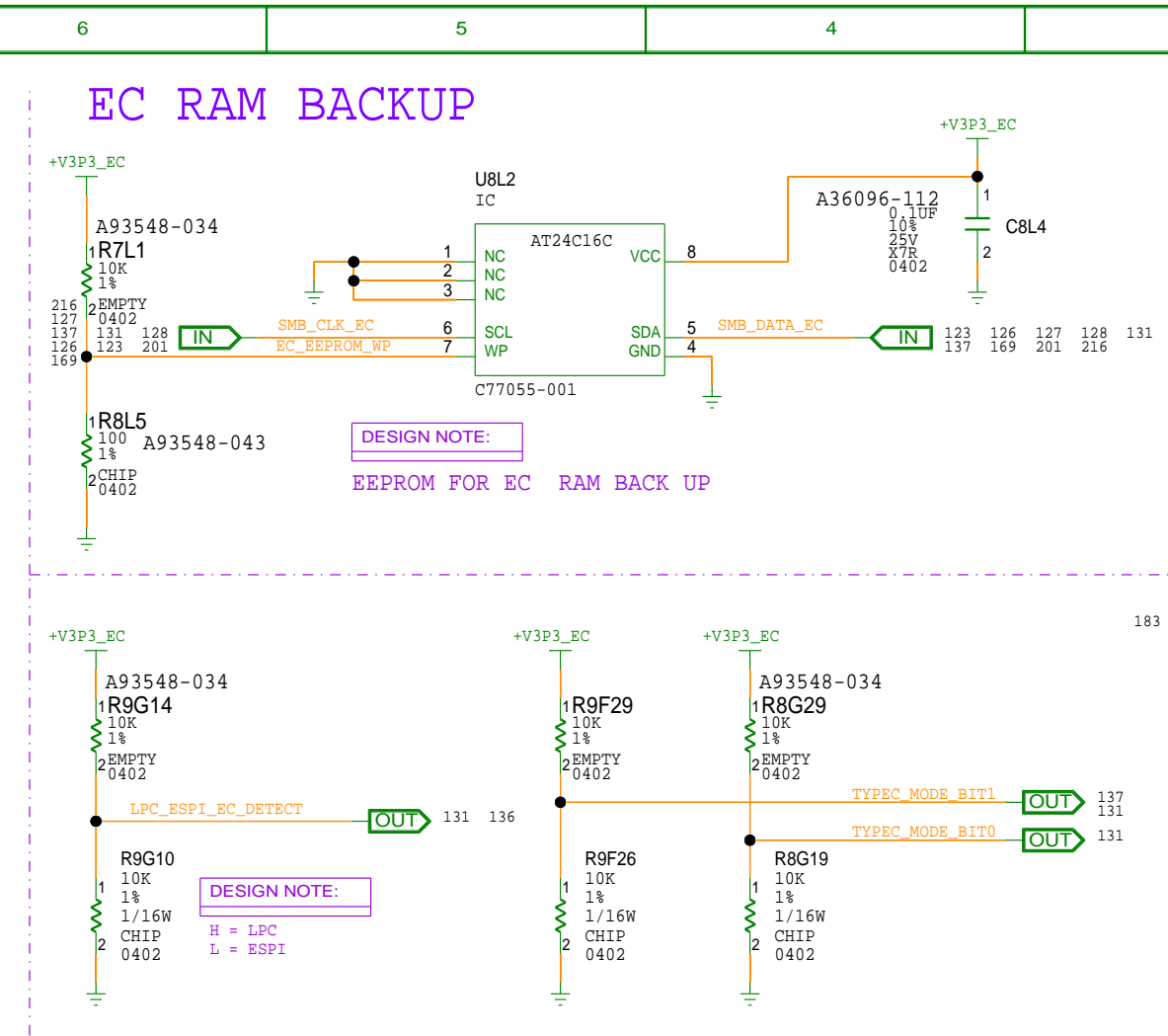
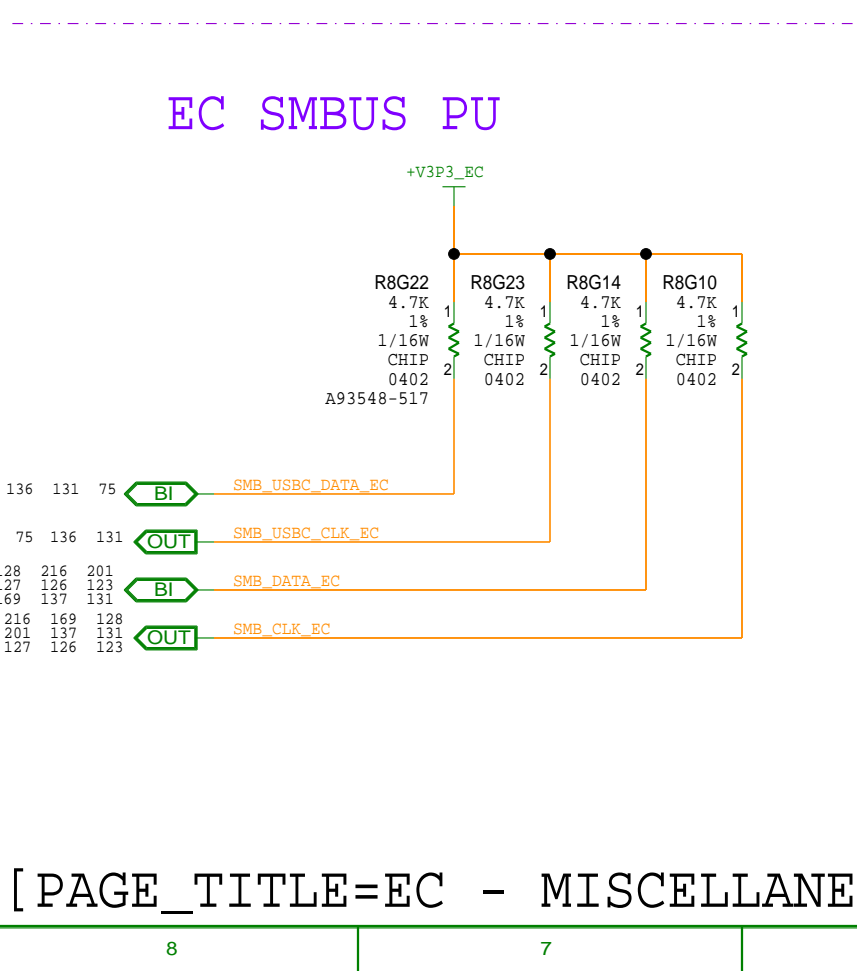
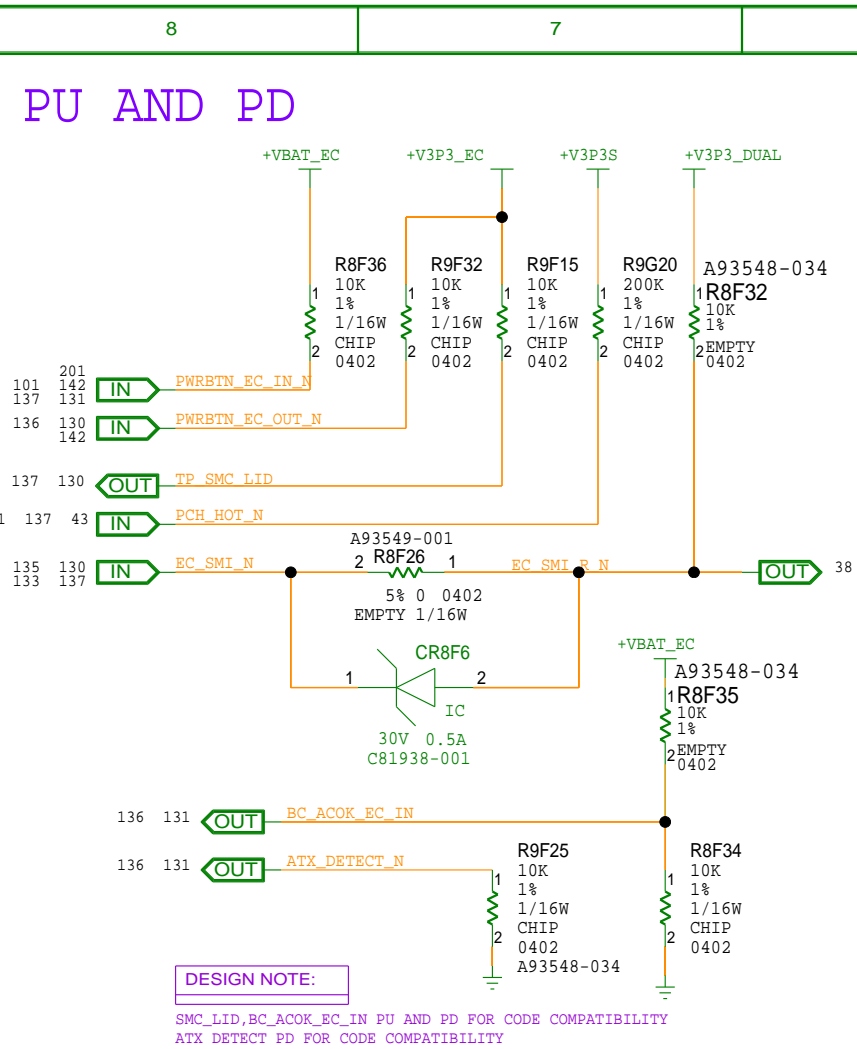


MODULE REV DETAILS

MODULE NAME	REV	DATE







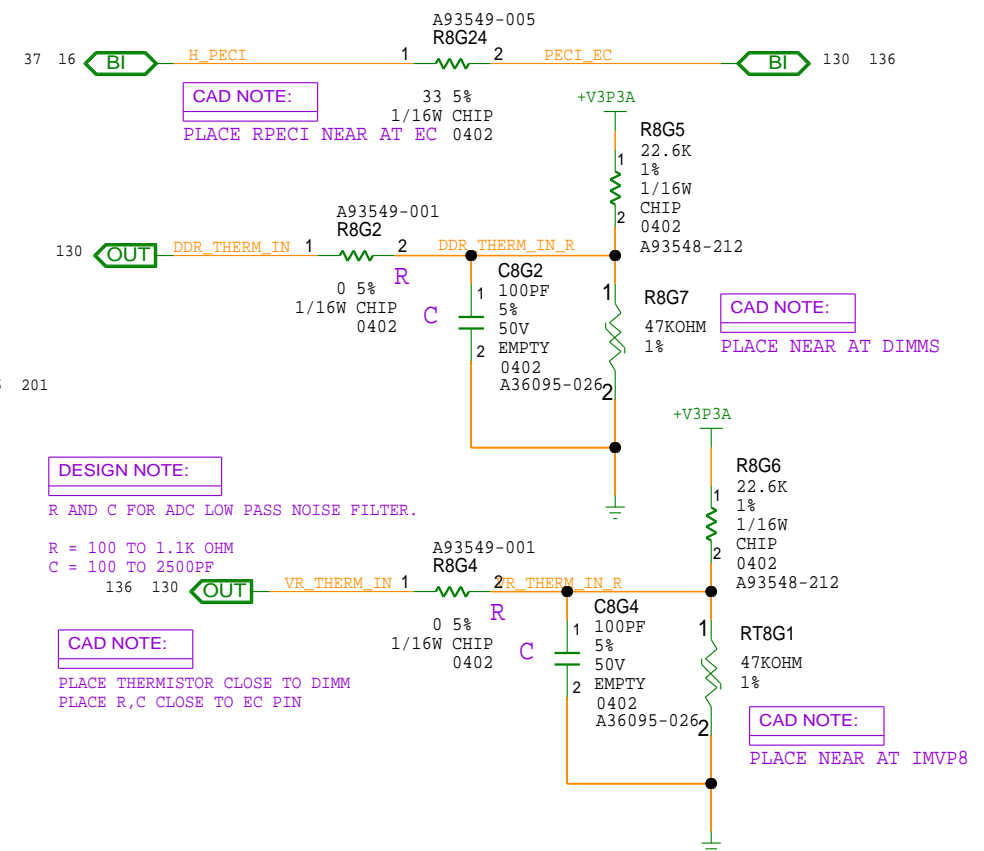
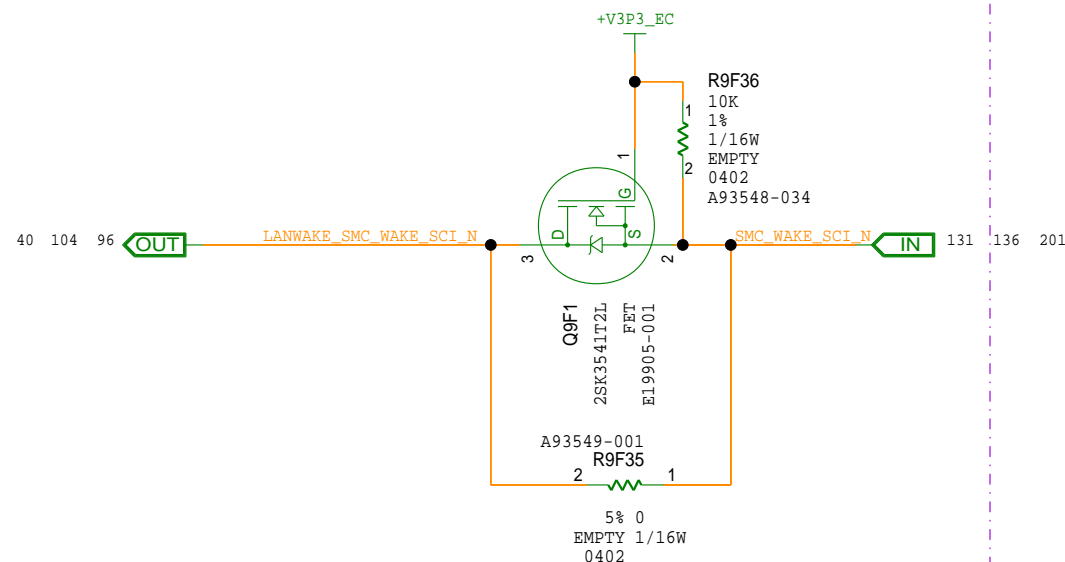
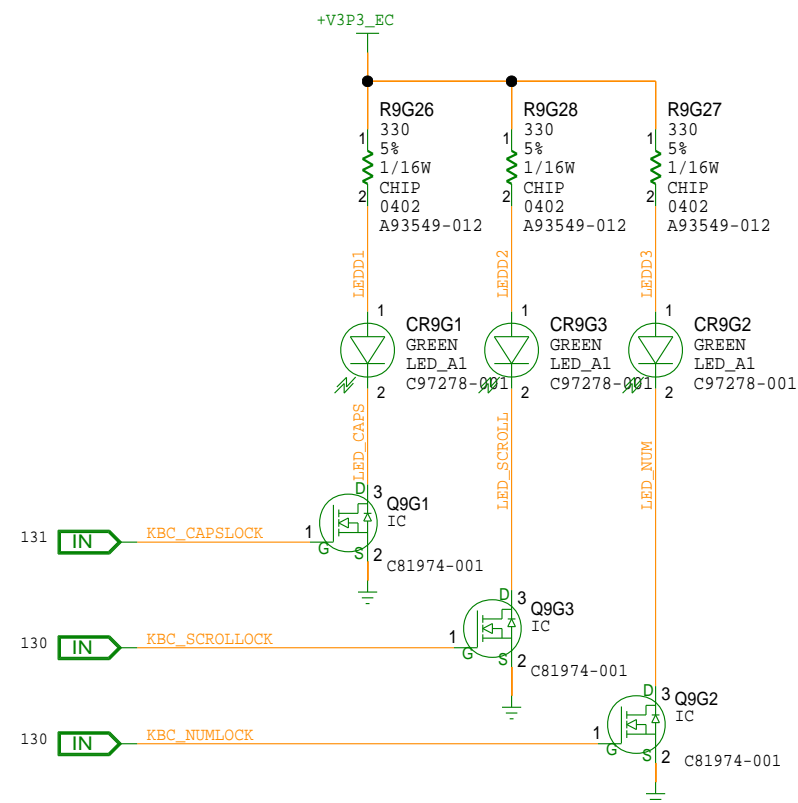




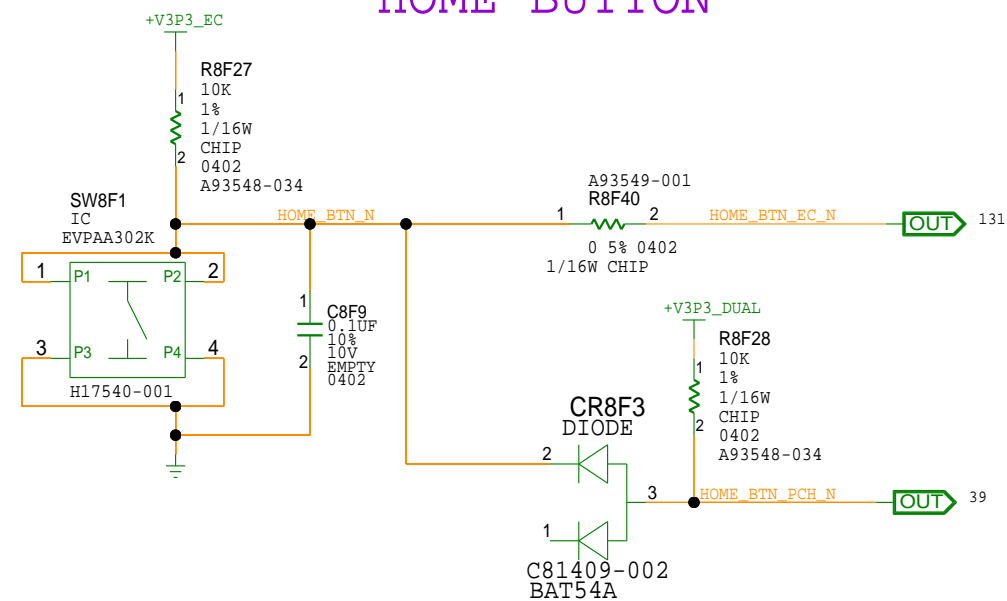
## THERMAL MANAGEMENT

## MODULE REV DETAILS

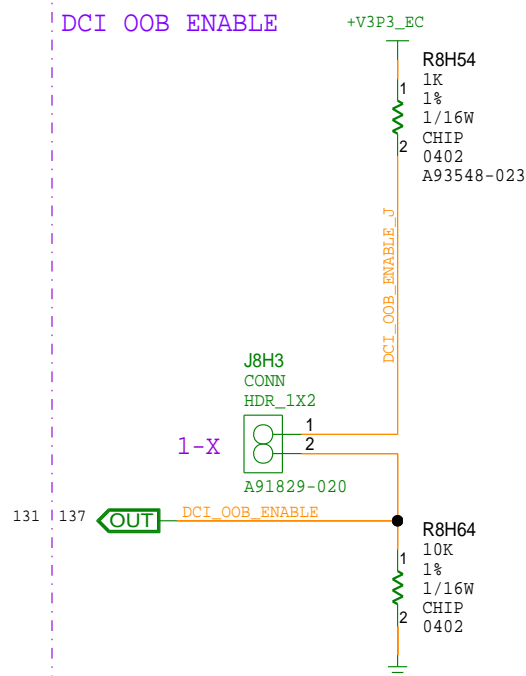
MODULE NAME	REV	DATE



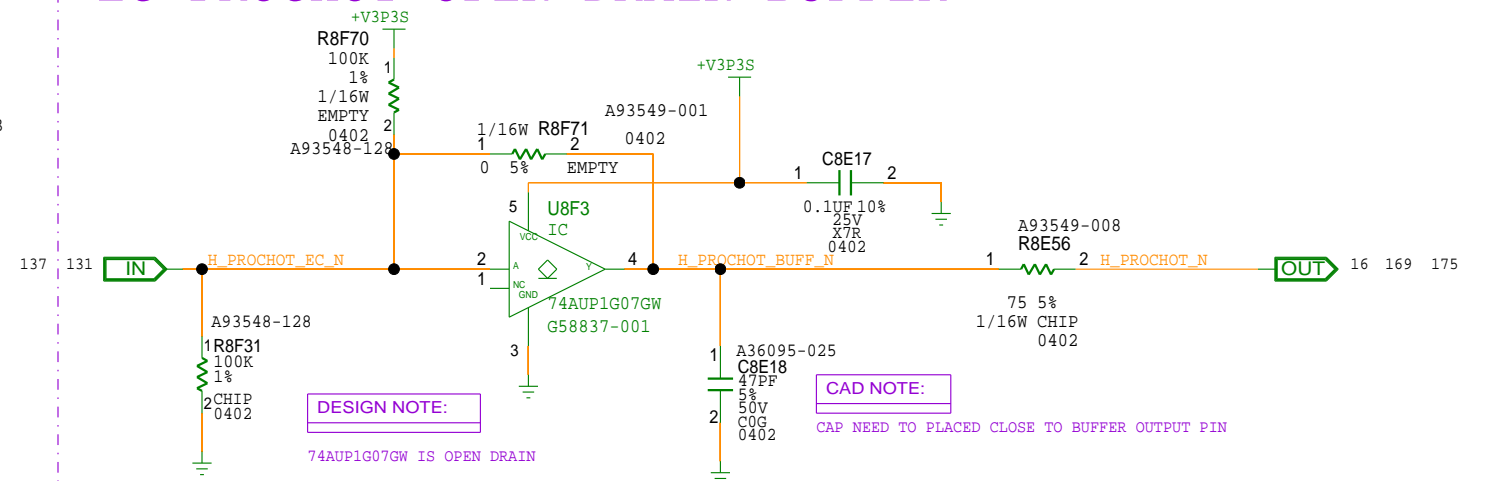
HOME    [BUTTON](#)



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! DCI_OOB_ENABLE
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## EC PROCHOT OPEN-DRAIN BUFFER



[PAGE\_TITLE=EC - MISCELLANEOUS - 2]

BPAGE DRAWING

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Fri Sep 27 16:41:17 2019

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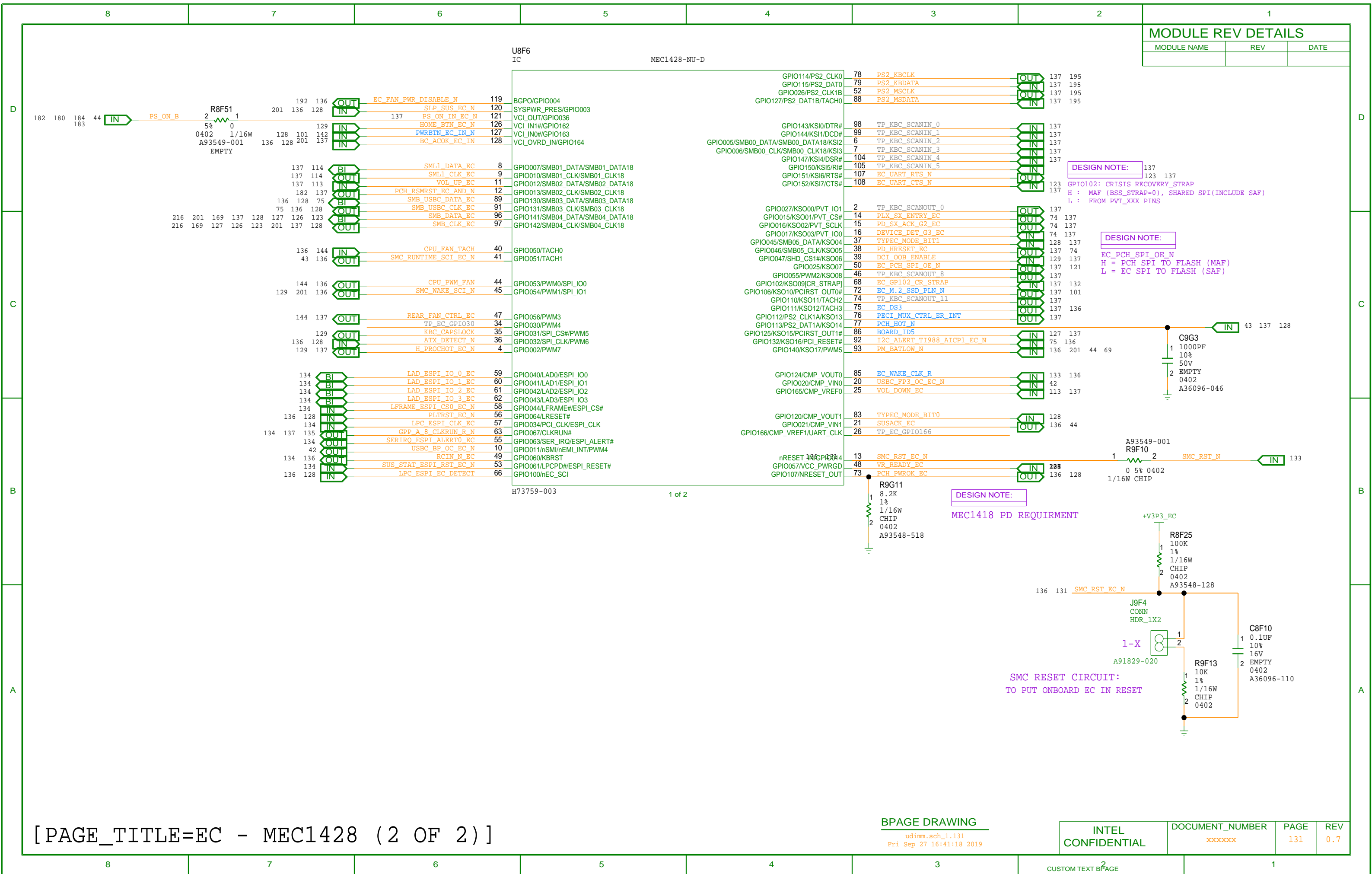
This diagram illustrates the electrical schematic for the EC power well section of the MEC14128 module, specifically page 130 of the drawing.

The central component is the U8F6 IC (MEC1428-NU-D), which interfaces with various external components and provides signals to other modules.

**Key Components and Connections:**

- U8F6 IC (MEC1428-NU-D):** The main controller chip, showing pins for I/O, power, and status signals.
- EC Power Well Section:** Includes components like R8G25, C8G7, and VREF\_CPU, connected to +V3P3\_EC and +VREF\_CPU.
- Voltage Level Straps:** Configured via VTR\_33\_18 and VTR\_33\_19, setting H (High) and L (Low) levels for VREF\_CPU.
- EC Power Well Section:** Shows connections for +V3P3A, +V3P3DSW, and +V3P3\_EC, along with resistors R8G26, R8G27, and capacitors C8F18, C8F19, C8F20, C8F21, C8F22, C8F23, C8F24, C8F25, C8F26, C8F27, C8F28, C8F29, C8F30, C8F31, C8F32, C8F33, C8F34, C8F35, C8F36, C8F37, C8F38, C8F39, C8F40, C8F41, C8F42, C8F43, C8F44, C8F45, C8F46, C8F47, C8F48, C8F49, C8F50, C8F51, C8F52, C8F53, C8F54, C8F55, C8F56, C8F57, C8F58, C8F59, C8F60, C8F61, C8F62, C8F63, C8F64, C8F65, C8F66, C8F67, C8F68, C8F69, C8F70, C8F71, C8F72, C8F73, C8F74, C8F75, C8F76, C8F77, C8F78, C8F79, C8F80, C8F81, C8F82, C8F83, C8F84, C8F85, C8F86, C8F87, C8F88, C8F89, C8F90, C8F91, C8F92, C8F93, C8F94, C8F95, C8F96, C8F97, C8F98, C8F99, C8F100, C8F101, C8F102, C8F103, C8F104, C8F105, C8F106, C8F107, C8F108, C8F109, C8F110, C8F111, C8F112, C8F113, C8F114, C8F115, C8F116, C8F117, C8F118, C8F119, C8F120, C8F121, C8F122, C8F123, C8F124, C8F125, C8F126, C8F127, C8F128, C8F129, C8F130, C8F131, C8F132, C8F133, C8F134, C8F135, C8F136, C8F137, C8F138, C8F139, C8F140, C8F141, C8F142, C8F143, C8F144, C8F145, C8F146, C8F147, C8F148, C8F149, C8F150, C8F151, C8F152, C8F153, C8F154, C8F155, C8F156, C8F157, C8F158, C8F159, C8F160, C8F161, C8F162, C8F163, C8F164, C8F165, C8F166, C8F167, C8F168, C8F169, C8F170, C8F171, C8F172, C8F173, C8F174, C8F175, C8F176, C8F177, C8F178, C8F179, C8F180, C8F181, C8F182, C8F183, C8F184, C8F185, C8F186, C8F187, C8F188, C8F189, C8F190, C8F191, C8F192, C8F193, C8F194, C8F195, C8F196, C8F197, C8F198, C8F199, C8F200, C8F201, C8F202, C8F203, C8F204, C8F205, C8F206, C8F207, C8F208, C8F209, C8F210, C8F211, C8F212, C8F213, C8F214, C8F215, C8F216, C8F217, C8F218, C8F219, C8F220, C8F221, C8F222, C8F223, C8F224, C8F225, C8F226, C8F227, C8F228, C8F229, C8F230, C8F231, C8F232, C8F233, C8F234, C8F235, C8F236, C8F237, C8F238, C8F239, C8F240, C8F241, C8F242, C8F243, C8F244, C8F245, C8F246, C8F247, C8F248, C8F249, C8F250, C8F251, C8F252, C8F253, C8F254, C8F255, C8F256, C8F257, C8F258, C8F259, C8F260, C8F261, C8F262, C8F263, C8F264, C8F265, C8F266, C8F267, C8F268, C8F269, C8F270, C8F271, C8F272, C8F273, C8F274, C8F275, C8F276, C8F277, C8F278, C8F279, C8F280, C8F281, C8F282, C8F283, C8F284, C8F285, C8F286, C8F287, C8F288, C8F289, C8F290, C8F291, C8F292, C8F293, C8F294, C8F295, C8F296, C8F297, C8F298, C8F299, C8F300, C8F301, C8F302, C8F303, C8F304, C8F305, C8F306, C8F307, C8F308, C8F309, C8F310, C8F311, C8F312, C8F313, C8F314, C8F315, C8F316, C8F317, C8F318, C8F319, C8F320, C8F321, C8F322, C8F323, C8F324, C8F325, C8F326, C8F327, C8F328, C8F329, C8F330, C8F331, C8F332, C8F333, C8F334, C8F335, C8F336, C8F337, C8F338, C8F339, C8F340, C8F341, C8F342, C8F343, C8F344, C8F345, C8F346, C8F347, C8F348, C8F349, C8F350, C8F351, C8F352, C8F353, C8F354, C8F355, C8F356, C8F357, C8F358, C8F359, C8F360, C8F361, C8F362, C8F363, C8F364, C8F365, C8F366, C8F367, C8F368, C8F369, C8F370, C8F371, C8F372, C8F373, C8F374, C8F375, C8F376, C8F377, C8F378, C8F379, C8F380, C8F381, C8F382, C8F383, C8F384, C8F385, C8F386, C8F387, C8F388, C8F389, C8F390, C8F391, C8F392, C8F393, C8F394, C8F395, C8F396, C8F397, C8F398, C8F399, C8F400, C8F401, C8F402, C8F403, C8F404, C8F405, C8F406, C8F407, C8F408, C8F409, C8F410, C8F411, C8F412, C8F413, C8F414, C8F415, C8F416, C8F417, C8F418, C8F419, C8F420, C8F421, C8F422, C8F423, C8F424, C8F425, C8F426, C8F427, C8F428, C8F429, C8F430, C8F431, C8F432, C8F433, C8F434, C8F435, C8F436, C8F437, C8F438, C8F439, C8F440, C8F441, C8F442, C8F443, C8F444, C8F445, C8F446, C8F447, C8F448, C8F449, C8F450, C8F451, C8F452, C8F453, C8F454, C8F455, C8F456, C8F457, C8F458, C8F459, C8F460, C8F461, C8F462, C8F463, C8F464, C8F465, C8F466, C8F467, C8F468, C8F469, C8F470, C8F471, C8F472, C8F473, C8F474, C8F475, C8F476, C8F477, C8F478, C8F479, C8F480, C8F481, C8F482, C8F483, C8F484, C8F485, C8F486, C8F487, C8F488, C8F489, C8F490, C8F491, C8F492, C8F493, C8F494, C8F495, C8F496, C8F497, C8F498, C8F499, C8F500, C8F501, C8F502, C8F503, C8F504, C8F505, C8F506, C8F507, C8F508, C8F509, C8F510, C8F511, C8F512, C8F513, C8F514, C8F515, C8F516, C8F517, C8F518, C8F519, C8F520, C8F521, C8F522, C8F523, C8F524, C8F525, C8F526, C8F527, C8F528, C8F529, C8F530, C8F531, C8F532, C8F533, C8F534, C8F535, C8F536, C8F537, C8F538, C8F539, C8F540, C8F541, C8F542, C8F543, C8F544, C8F545, C8F546, C8F547, C8F548, C8F549, C8F550, C8F551, C8F552, C8F553, C8F554, C8F555, C8F556, C8F557, C8F558, C8F559, C8F560, C8F561, C8F562, C8F563, C8F564, C8F565, C8F566, C8F567, C8F568, C8F569, C8F570, C8

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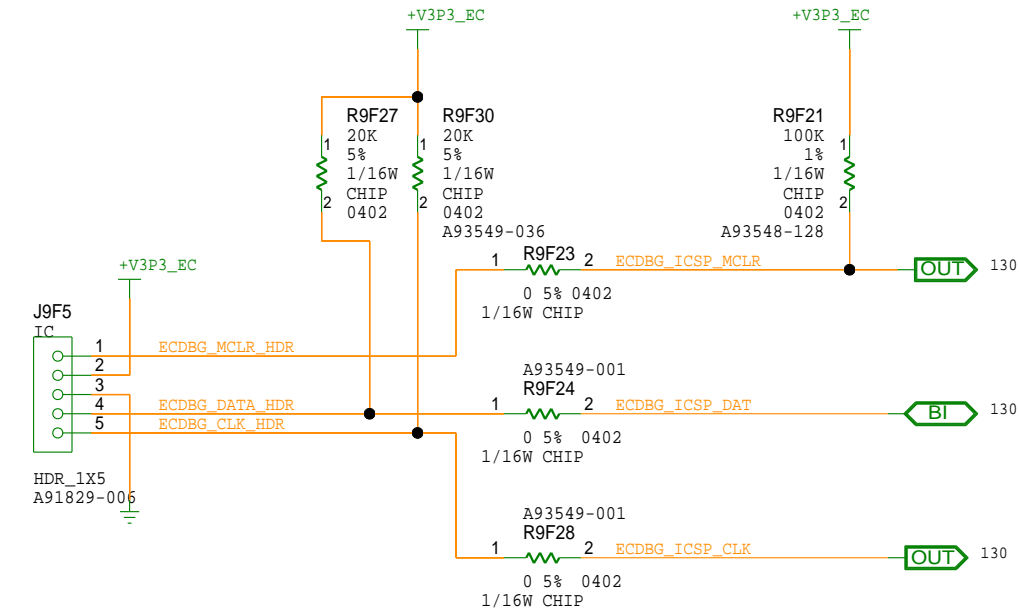




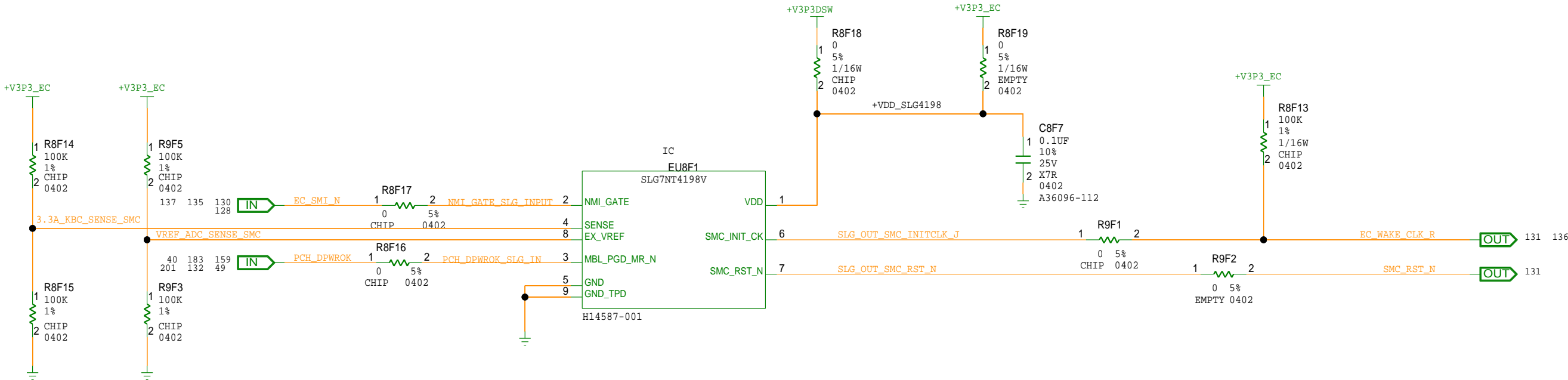
MODULE REV DETAILS

MODULE NAME	REV	DATE

ICSP DEBUG HEADER



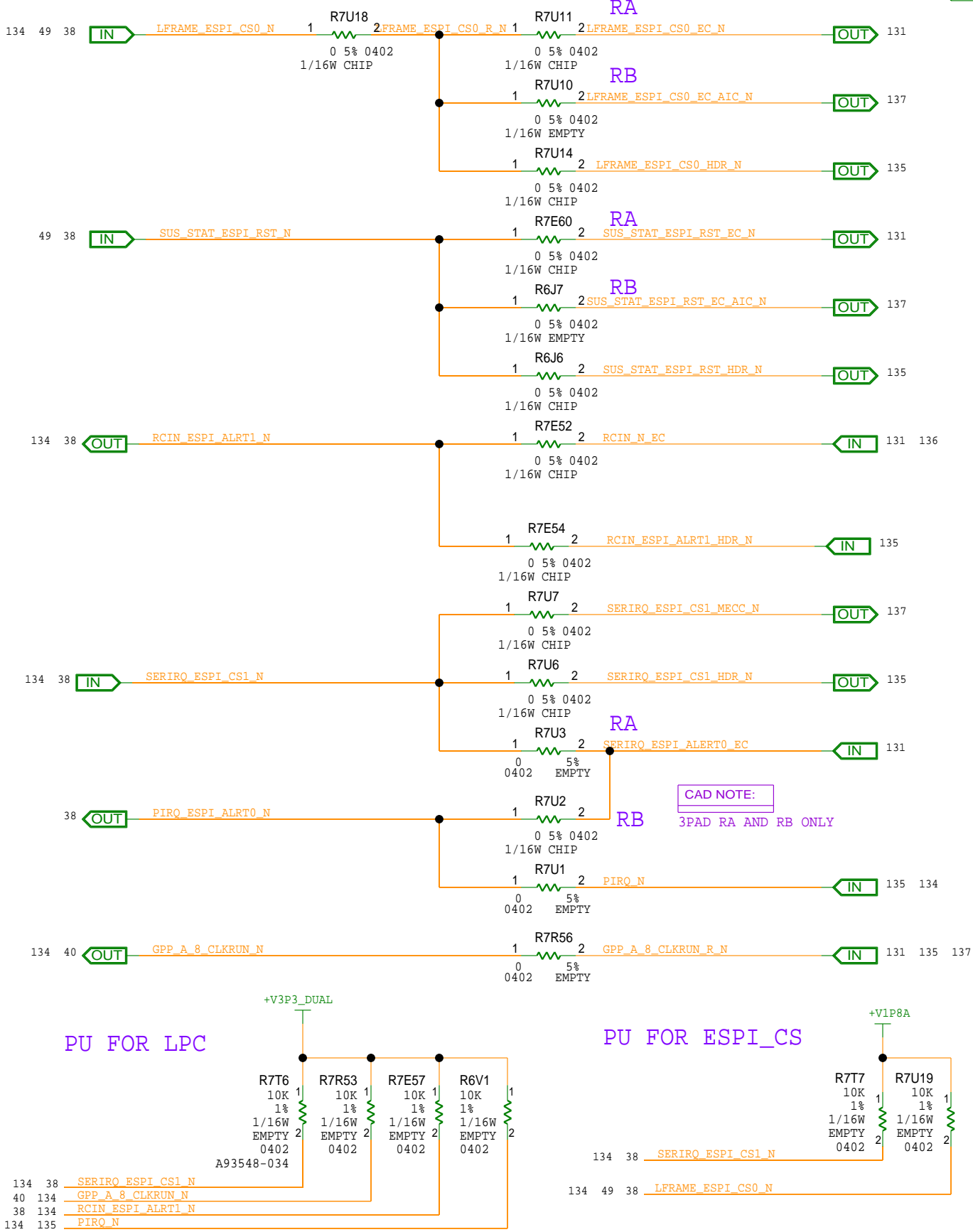
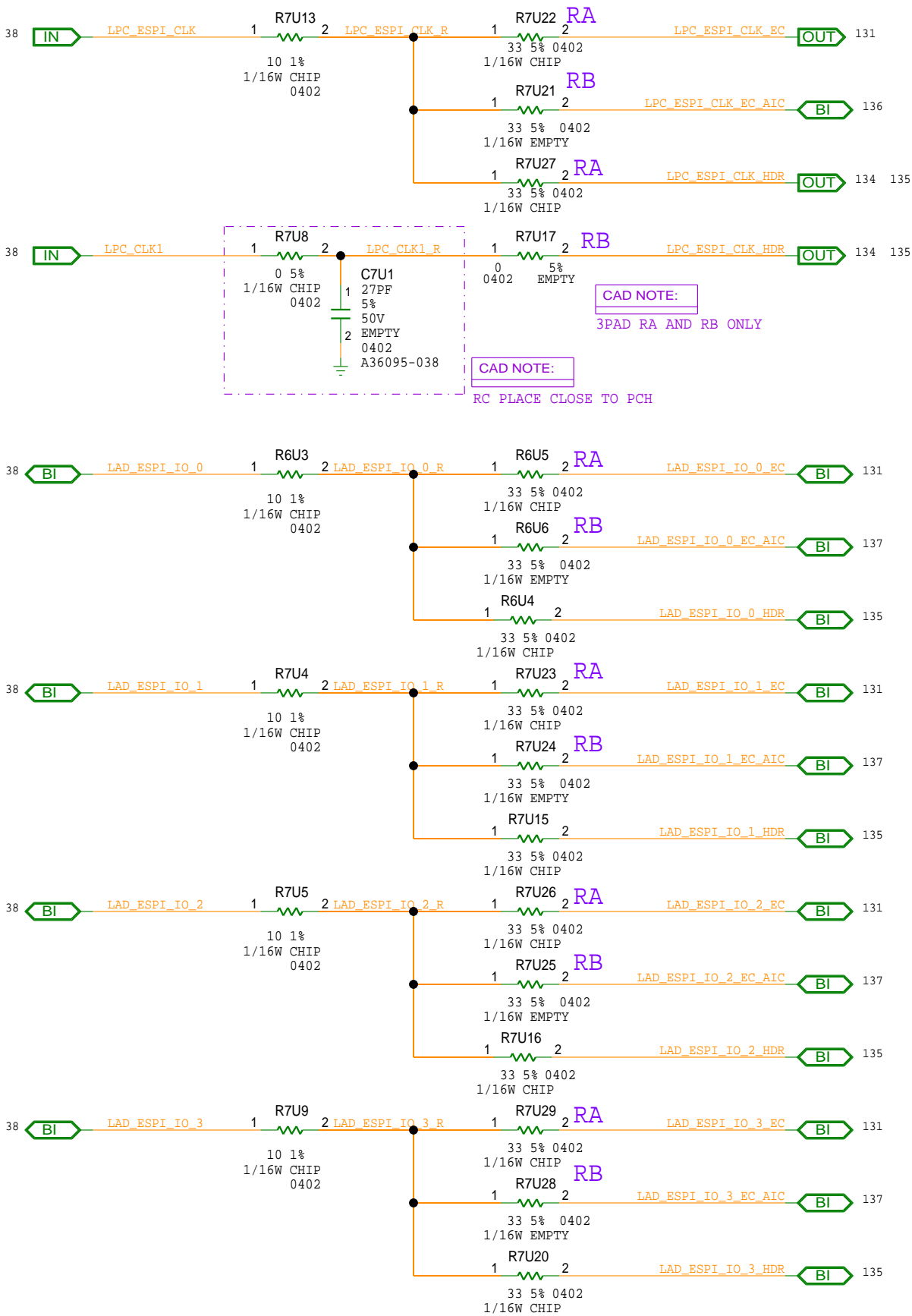
SMC\_RST\_N AND 1HZ CLOCK GENERATION



ESPI/LPC 2 LOAD TOPOLOGY (NOT TO 3PAD \*\_EC/\*\_HDR , ONLY 3PAD RA/RB)

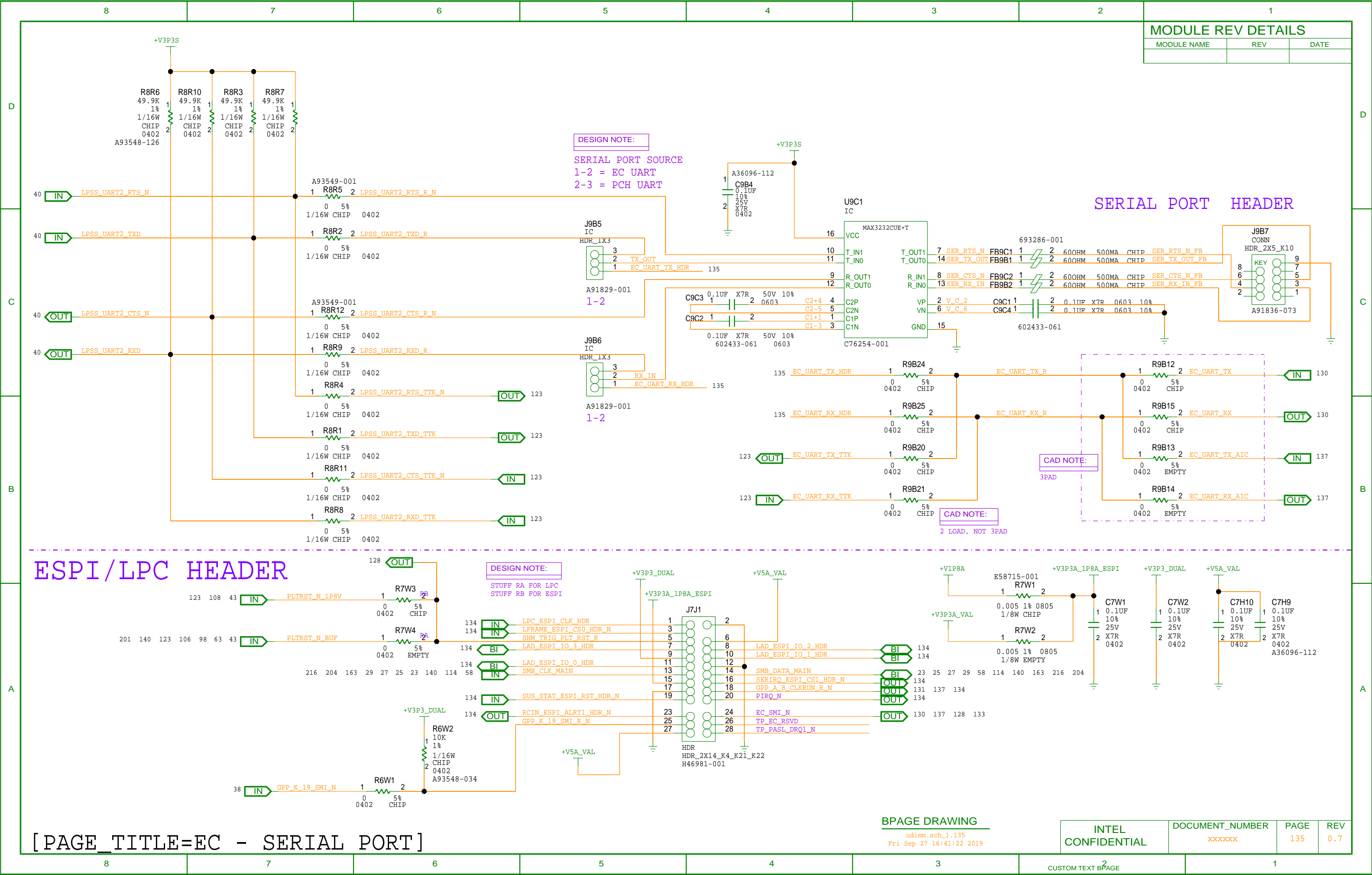
MODULE REV DETAILS

MODULE NAME	REV	DATE

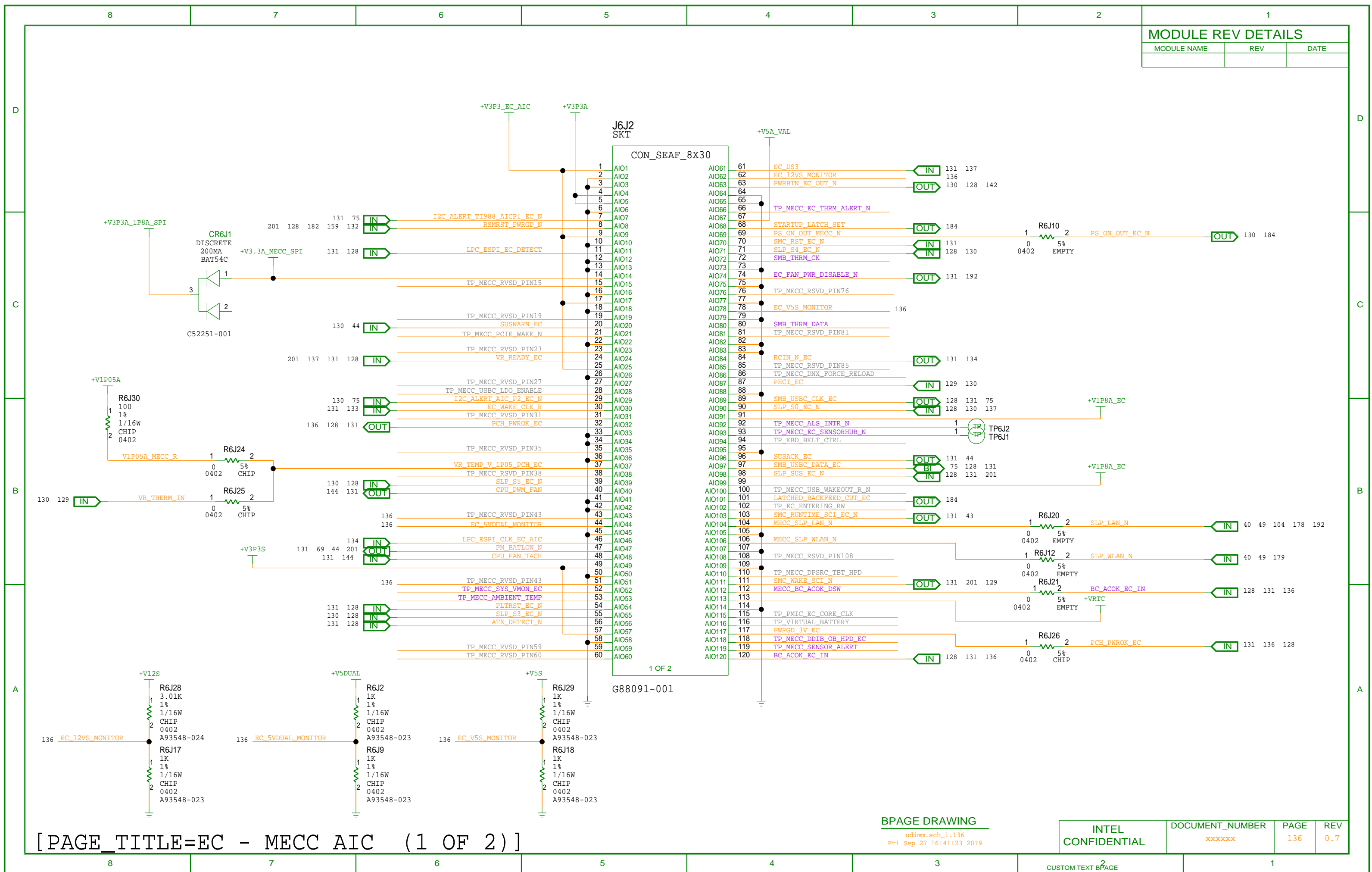


PU FOR LPC

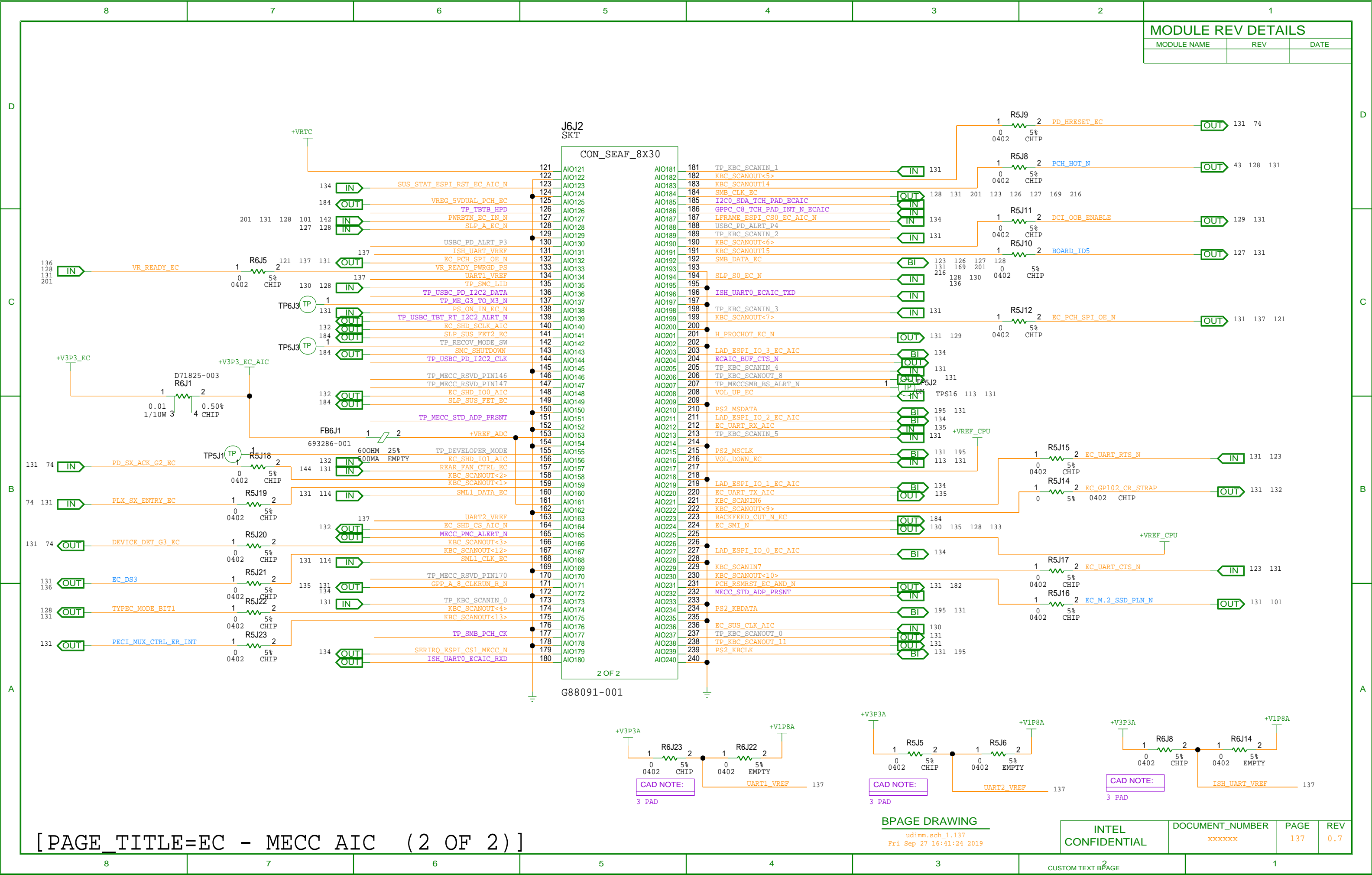
PU FOR ESPI\_CS











## D



A

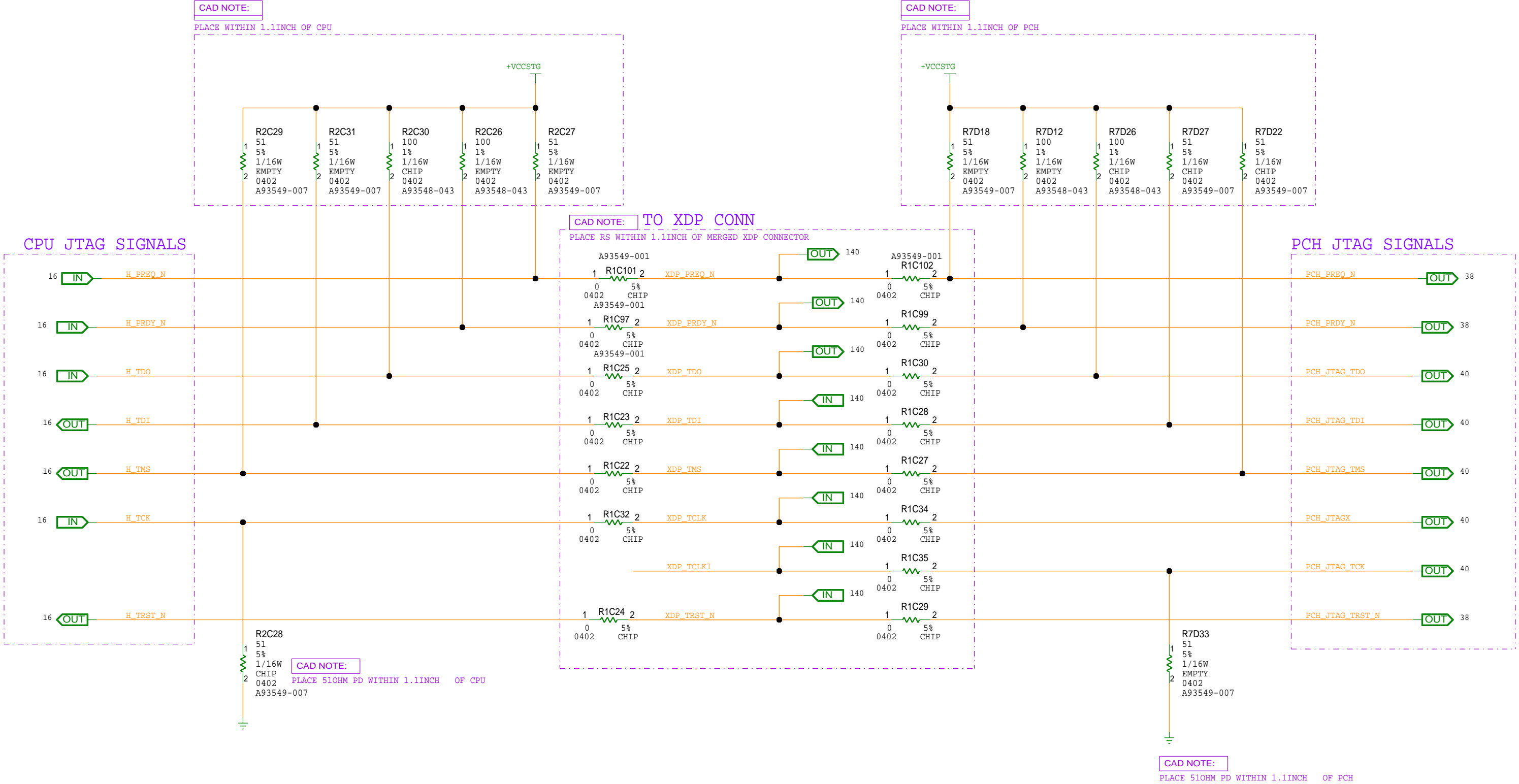
3	CUSTOM TEXT B PAGE	1
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138	0.7

MODULE REV DETAILS

MODULE NAME	REV	DATE

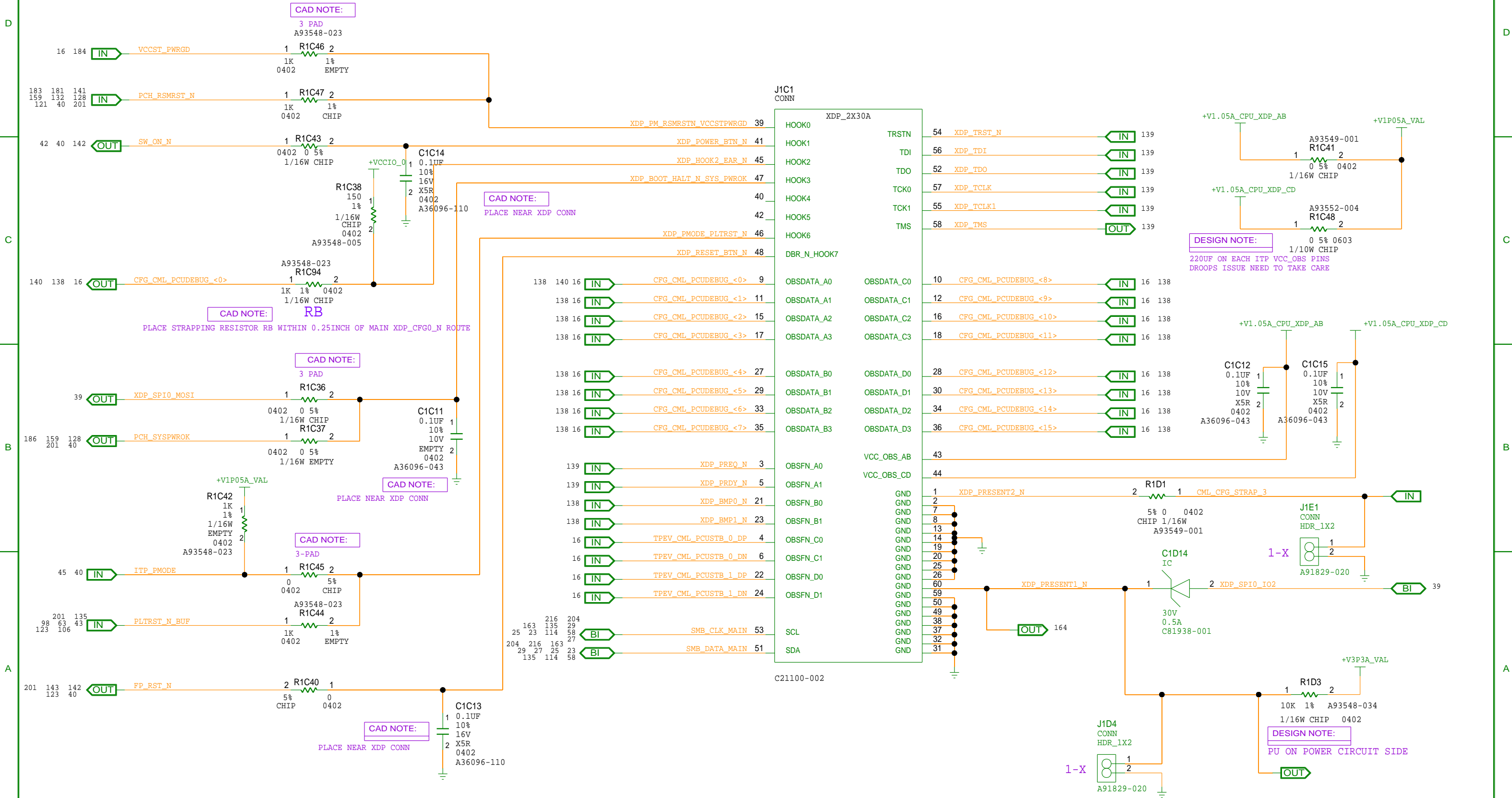
MERGED XDP JTAG SIGNALS



MERGED XDP CONNECTOR

MODULE REV DETAILS

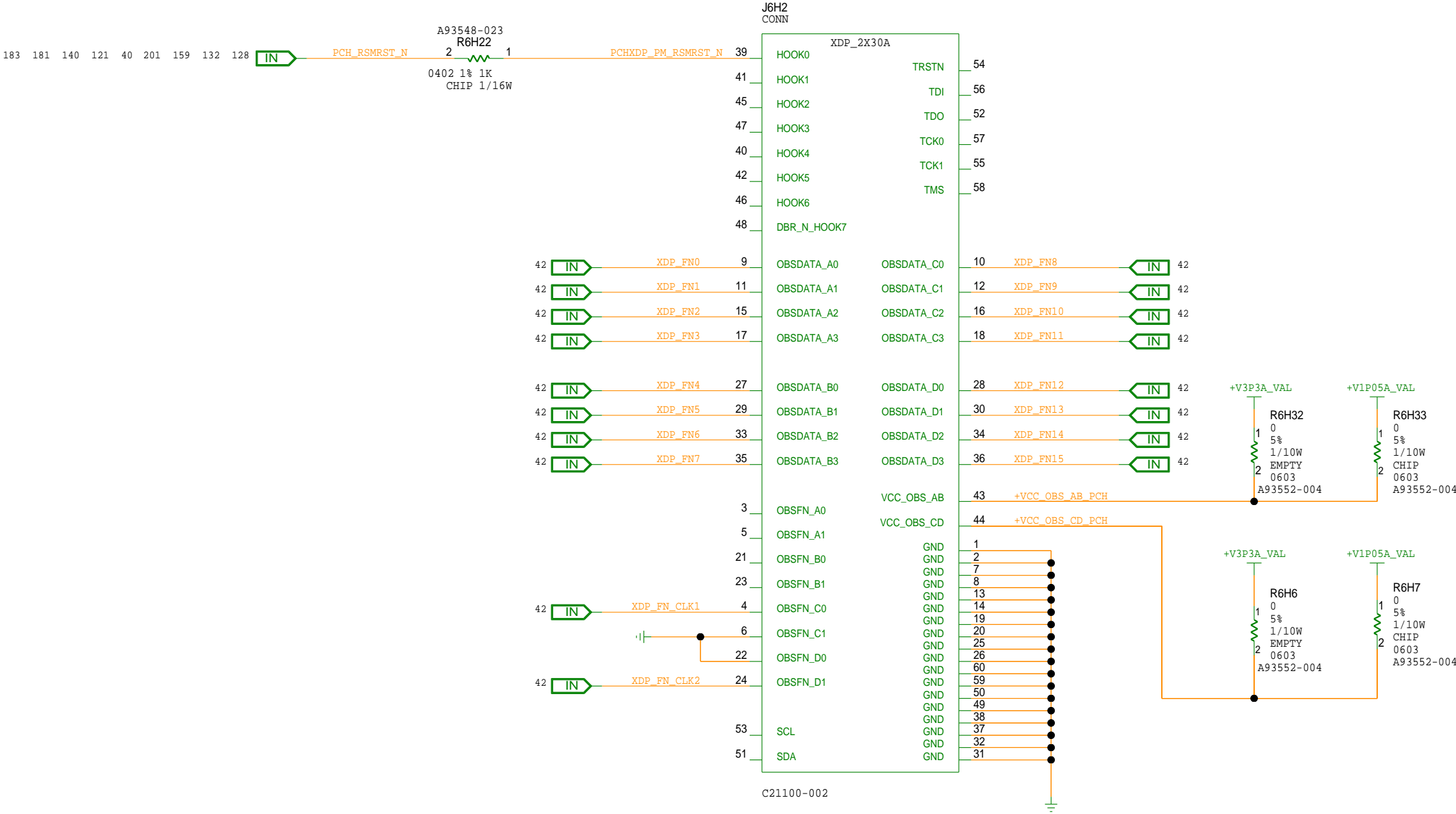
MODULE NAME	REV	DATE



MODULE REV DETAILS

MODULE NAME	REV	DATE

PCH VISA ONLY XDP CONNECTOR



[ PAGE\_TITLE=JTAG/CFG - JTAG/CFG - PCH VISA-ONLY XDP CONNECTOR ]

BPAGE DRAWING

udimm.sch\_1.141  
Fri Sep 27 16:41:27 2019

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DOCUMENT\_NUMBER

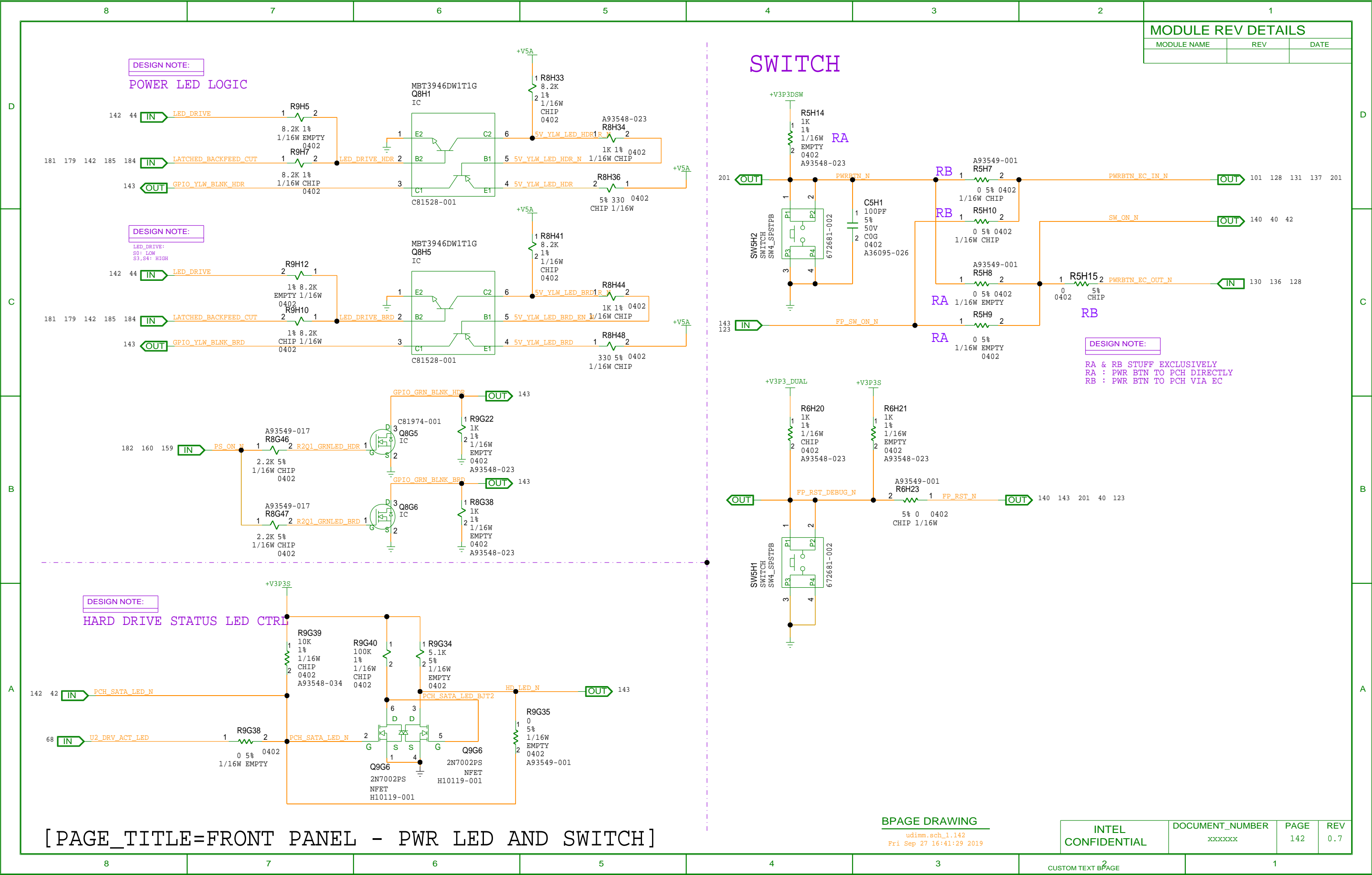
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141

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0.7



SWITCH

OUT

FP\_SW\_ON\_N

143

123

OUT

FP\_RST\_DEBUG\_N

140

143

201

40

123

RA & RB STUFF EXCLUSIVELY

RA : PWR BTN TO PCH DIRECTLY

RB : PWR BTN TO PCH VIA EC

BPAGE DRAWING

udimm.sch\_1.142

Fri Sep 27 16:41:29 2019

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CONFIDENTIAL

DOCUMENT\_NUMBER

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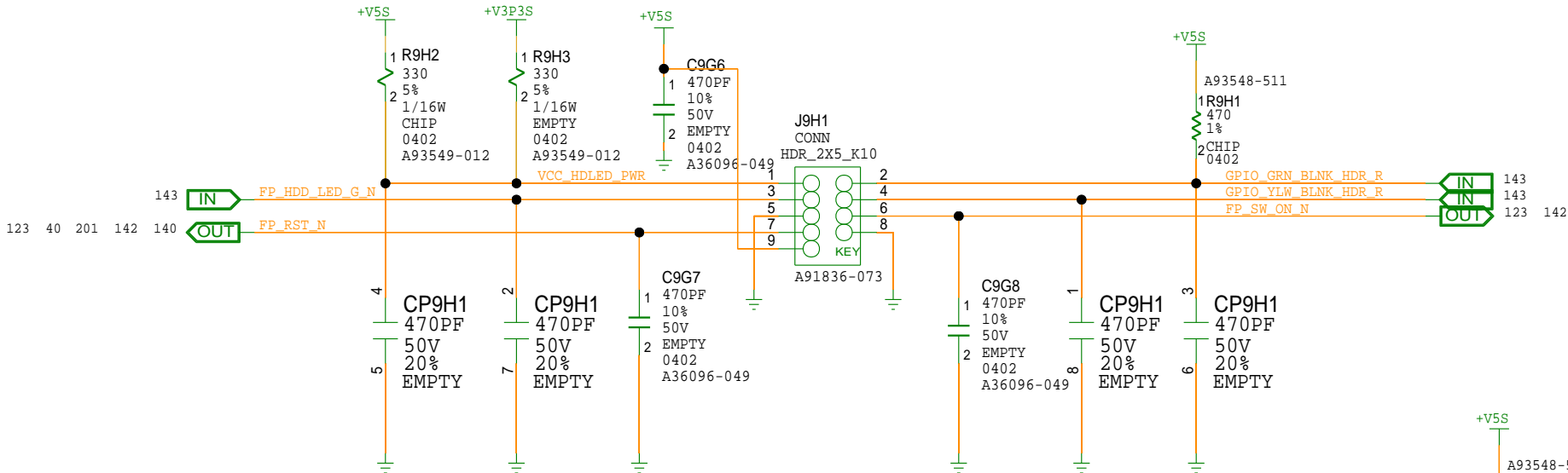
CUSTOM TEXT BPAGE

2

1

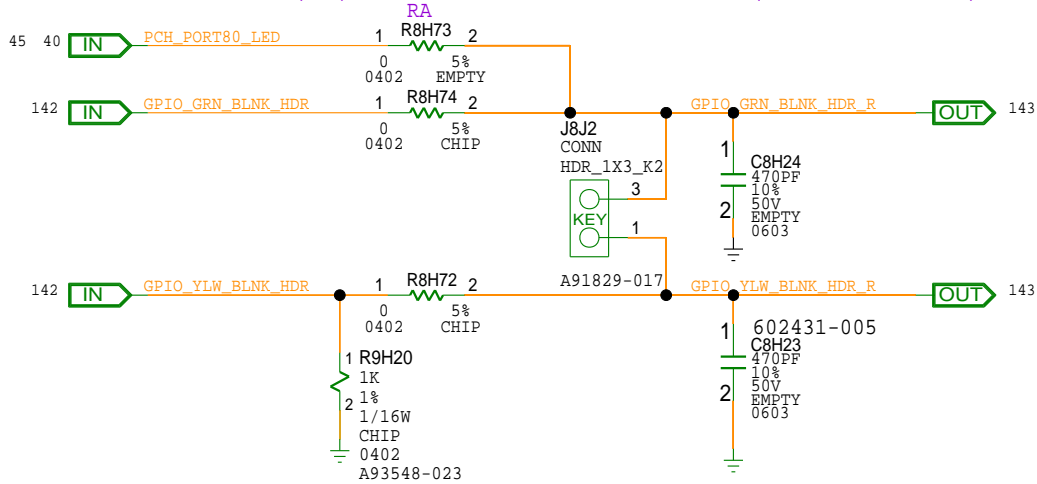
MODULE REV DETAILS

MODULE NAME	REV	DATE



BOM NOTE:

DEFAULT EMPTY: STUFF 0 OHM RES (RA) FOR PCH PORT80 LED FEATURE (TDE EXPERIMENT)

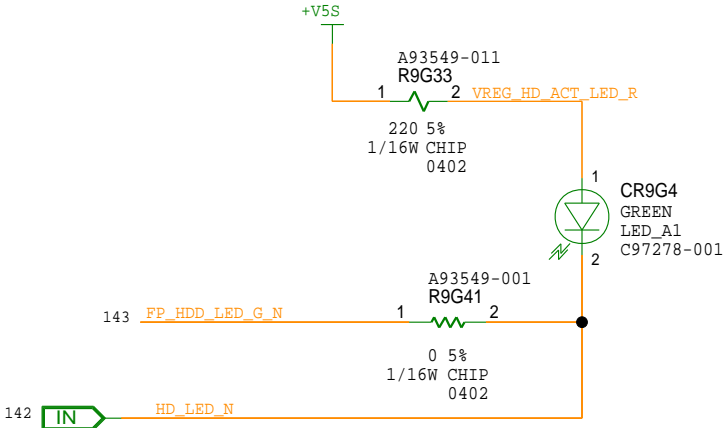
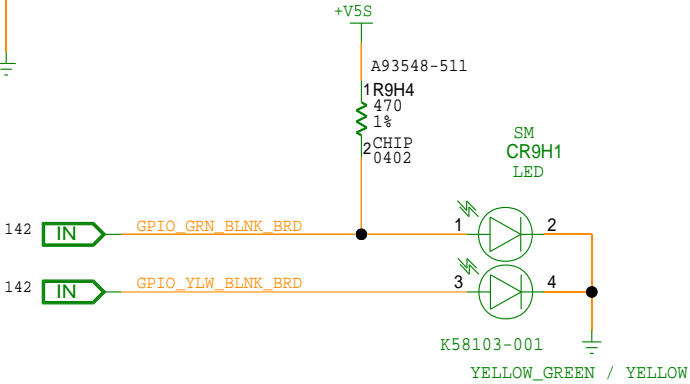


DESIGN NOTE:

S0: GREEN LIGHT  
S3: YELLOW LIGHT

CAD NOTE:

SILKSCREEN ON BRD: S0 = GREEN LIGHT, S3 = YELLOW LIGHT

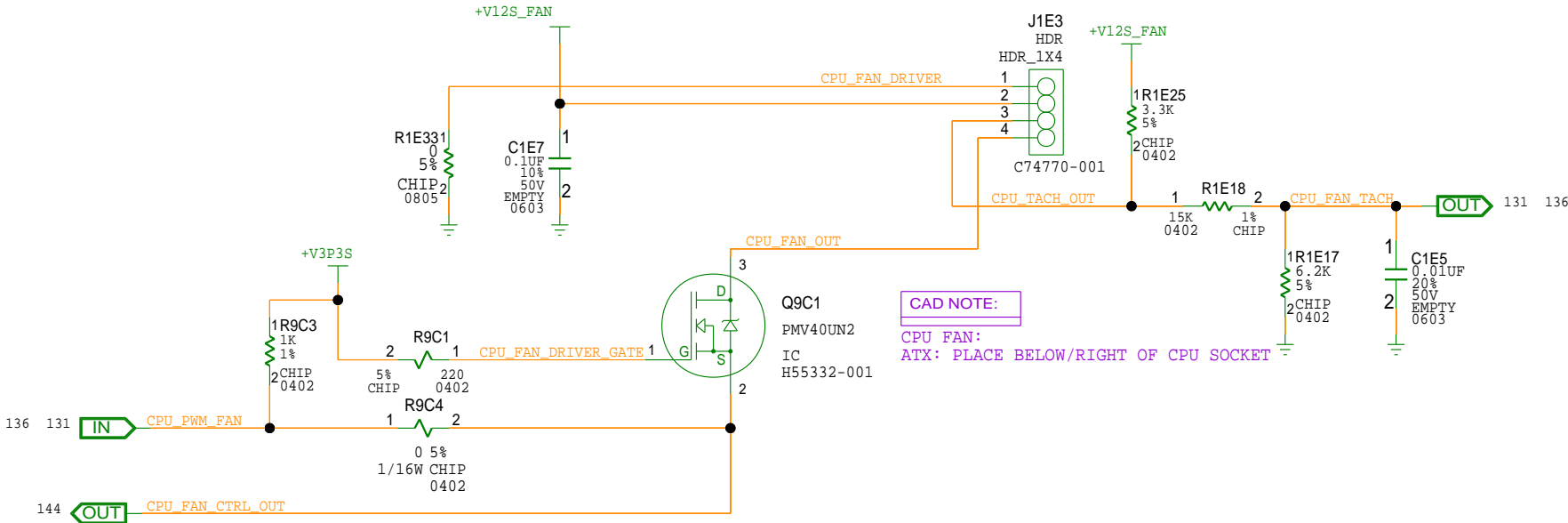




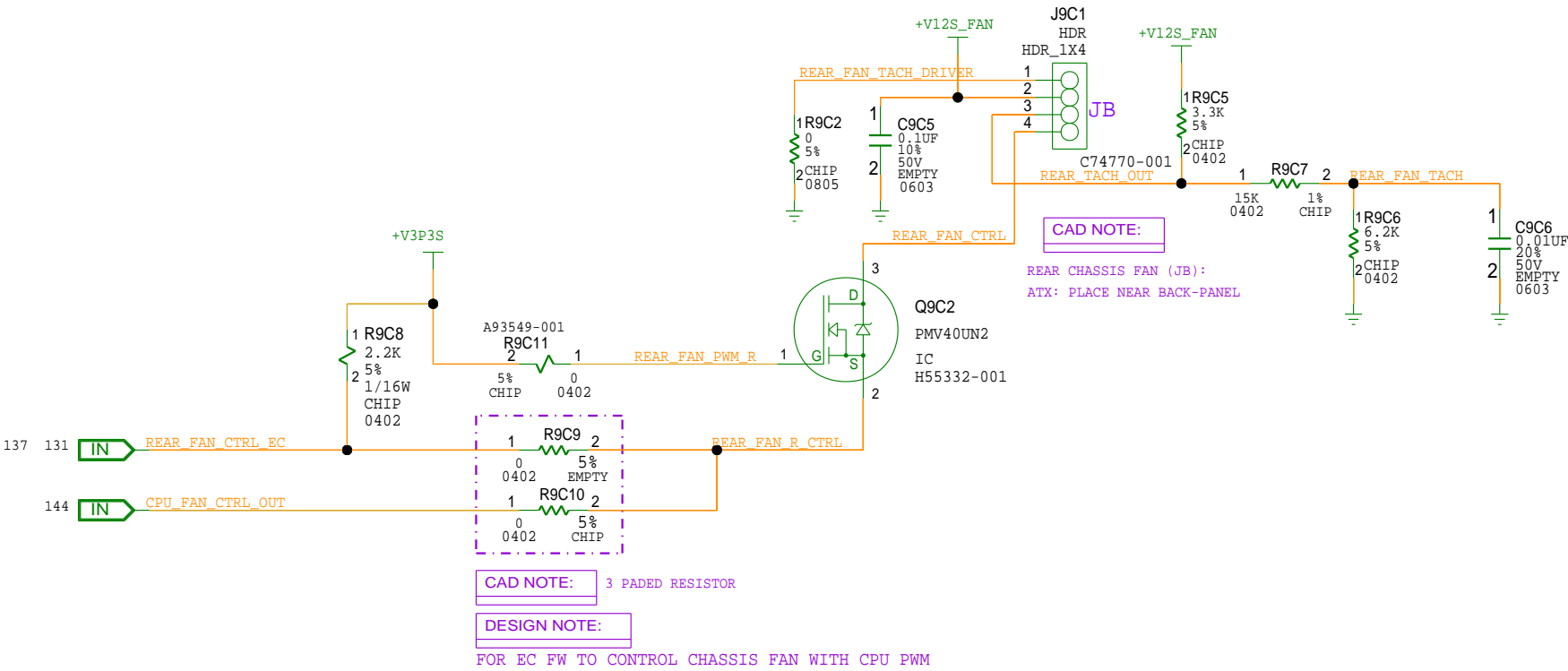
MODULE REV DETAILS

MODULE NAME	REV	DATE

CPU FAN HEADER

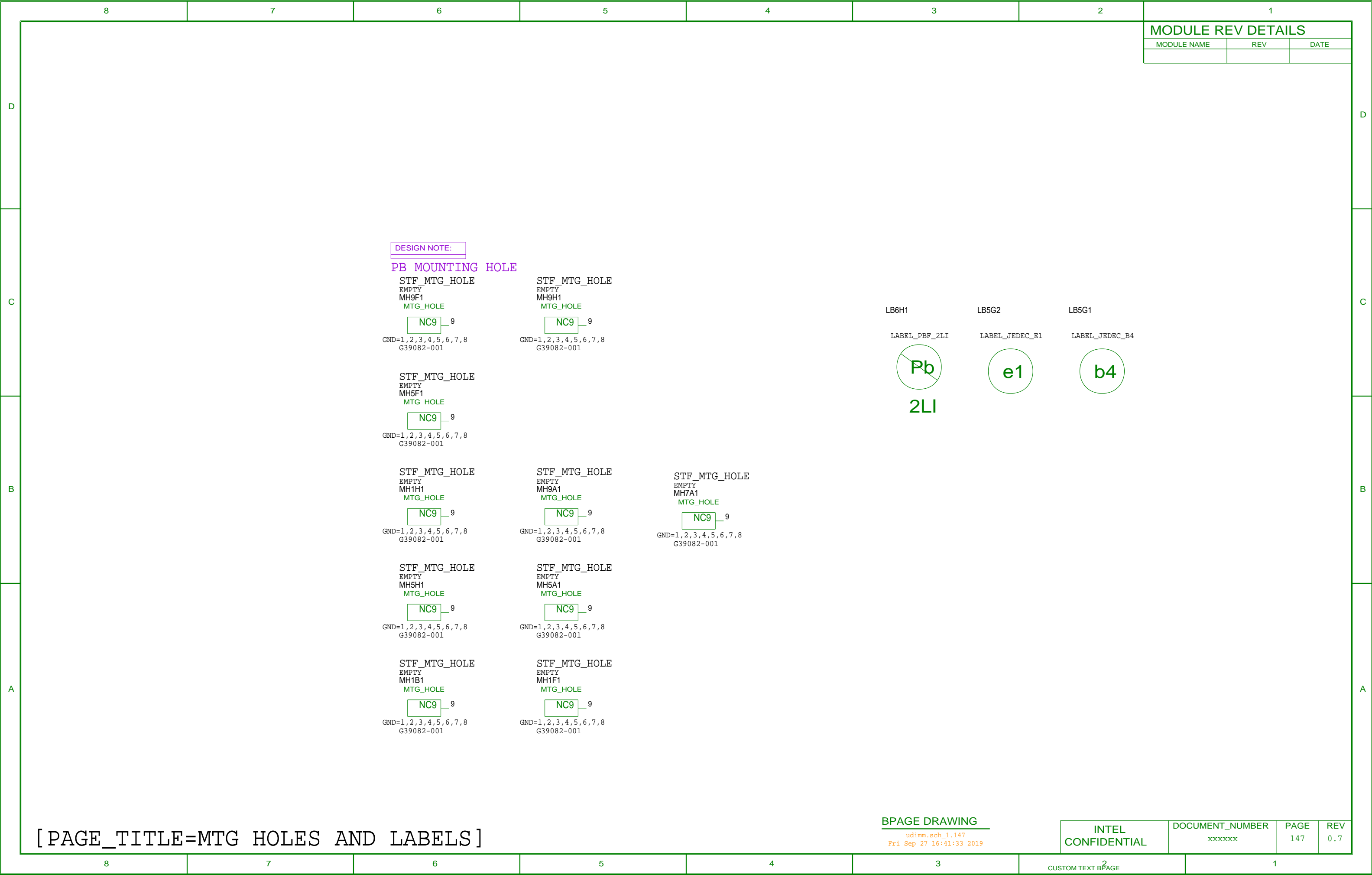


REAR CHASSIS FAN HEADER

















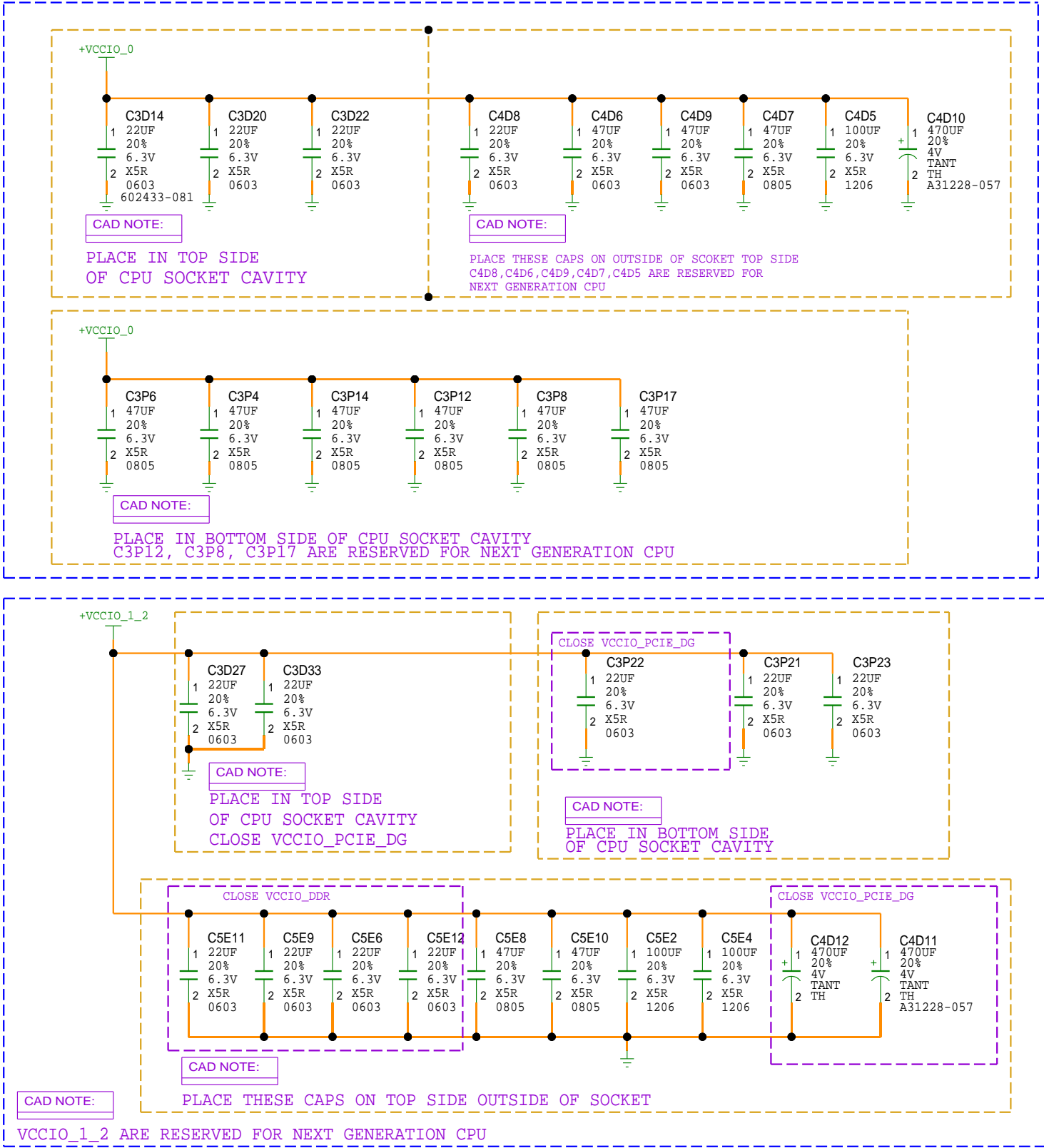
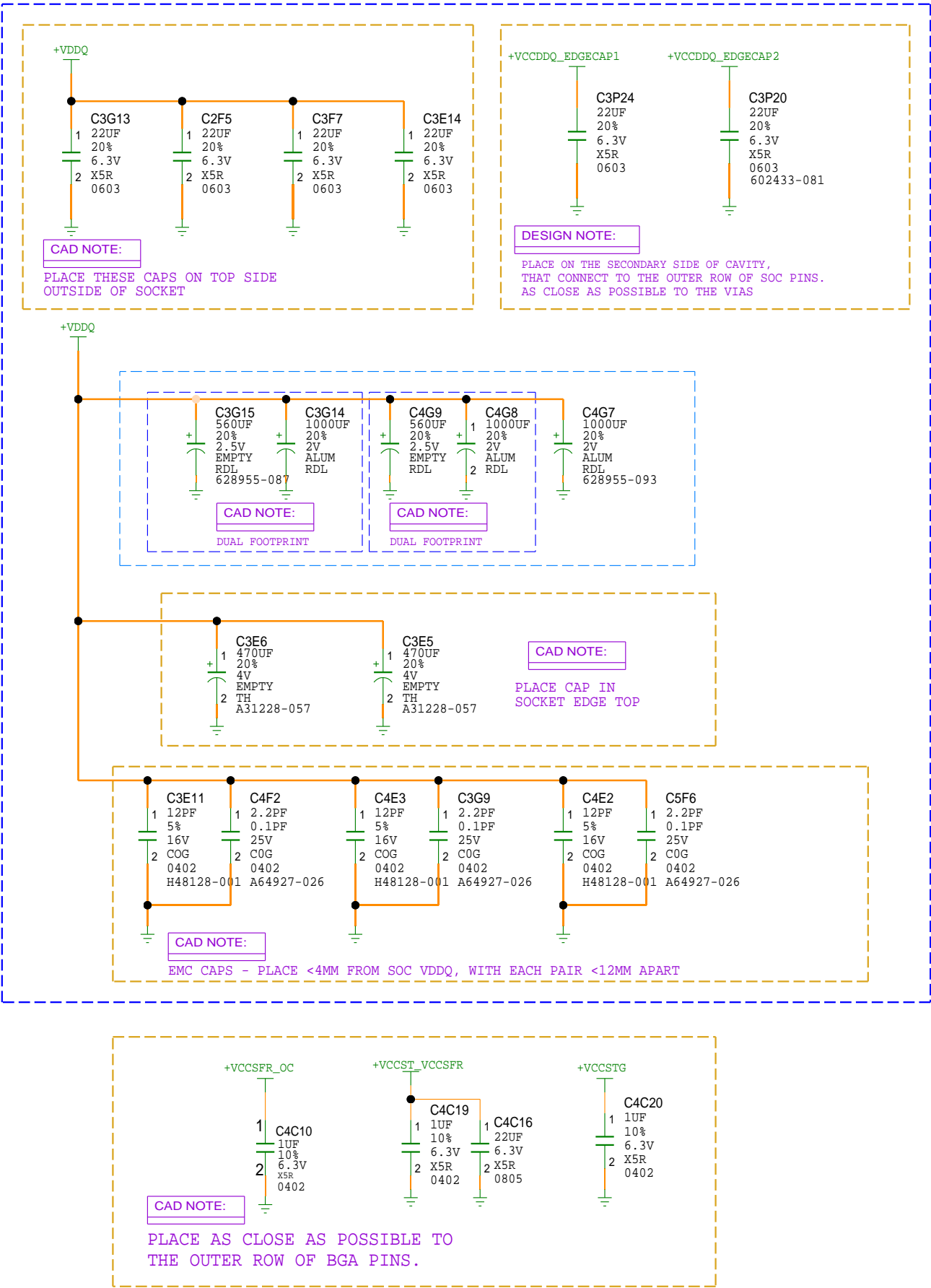






MODULE REV DETAILS

MODULE NAME	REV	DATE



[PAGE\_TITLE=CPU PD BOM-2 OF 2,VDDQ,VCCIO,VCCST\_VCCSFR,VCCSFR\_OC]

BPAGE DRAWING

udimm.sch\_1.154  
Fri Sep 27 16:41:38 2019

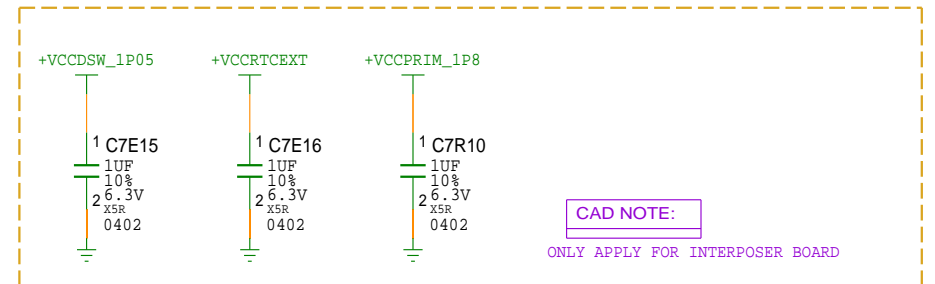
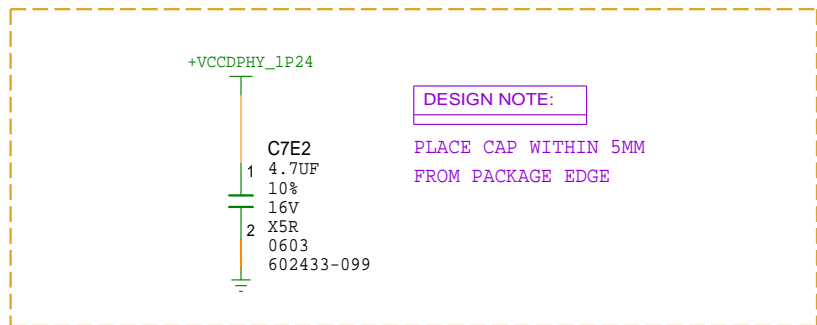
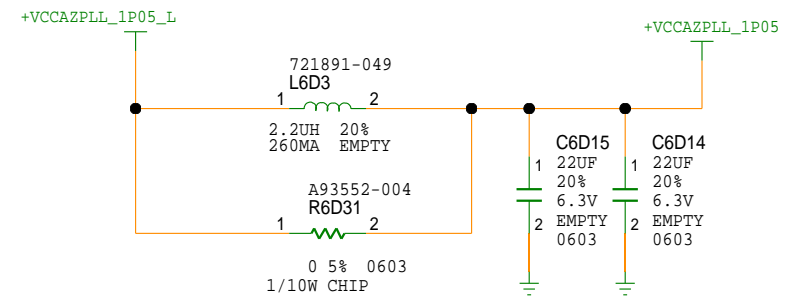
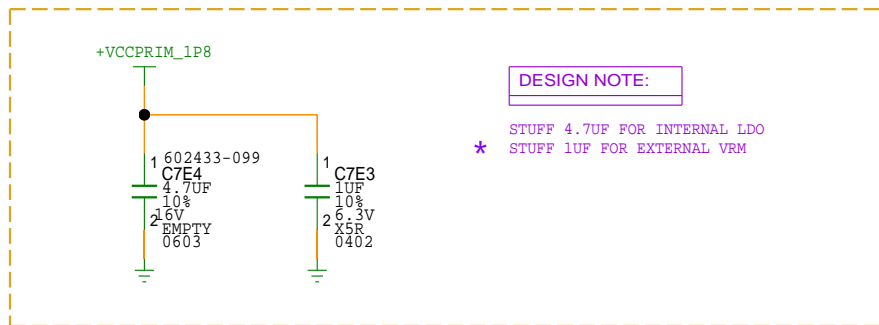
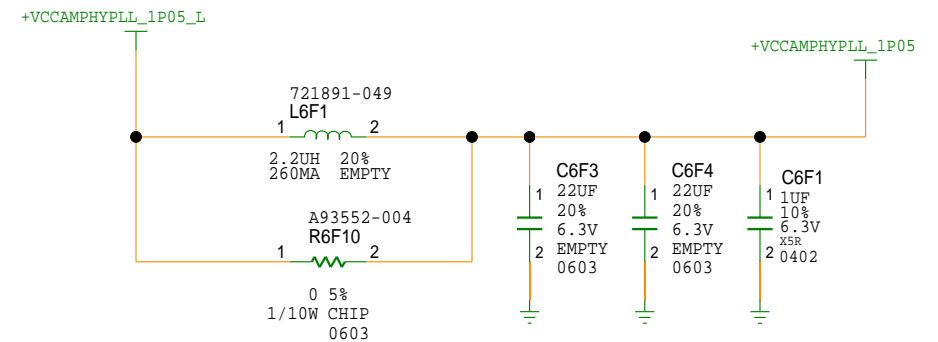
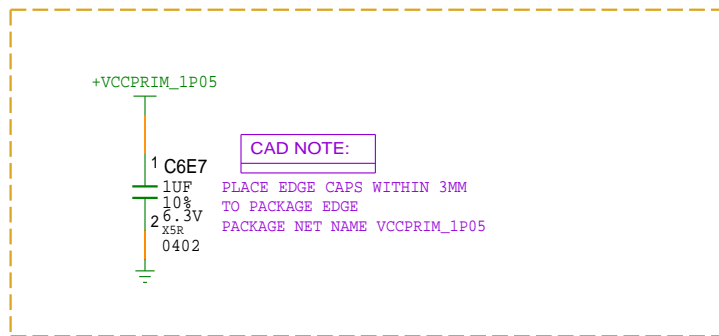
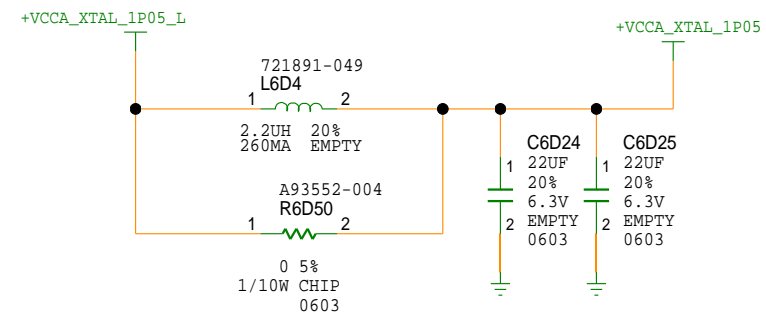
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udimm.sch\_1.155  
Fri Sep 27 16:41:39 2019

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DOCUMENT NUMBER

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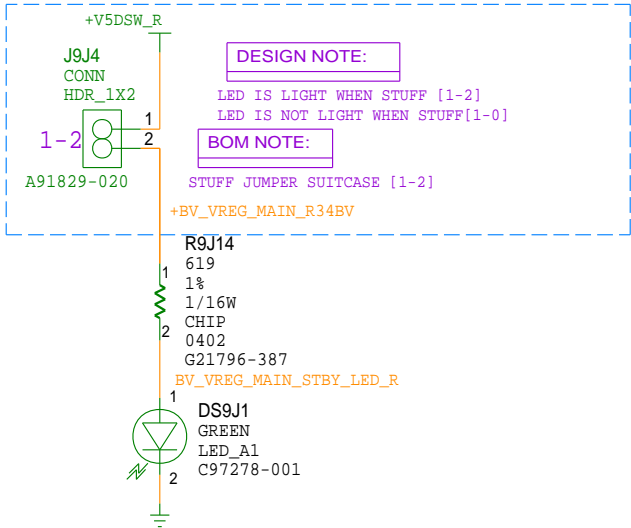
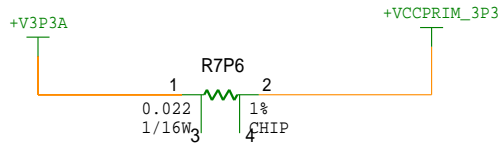
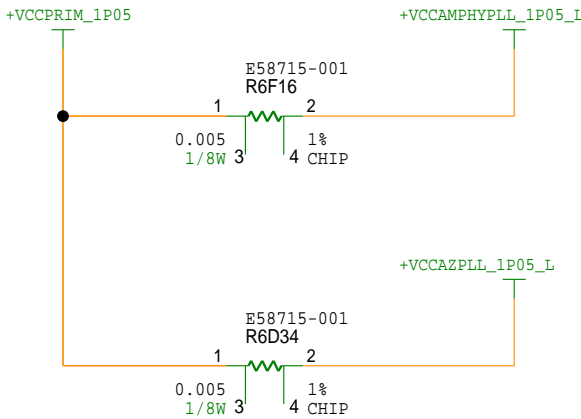
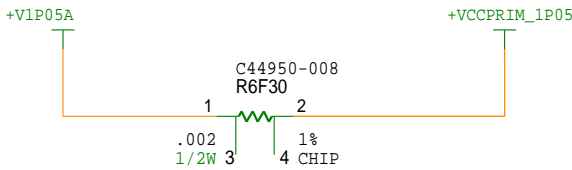
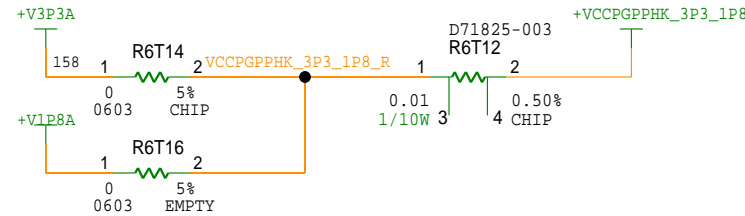
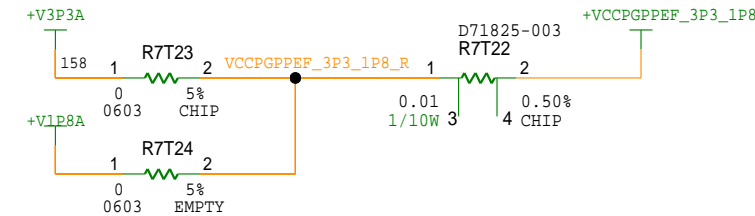
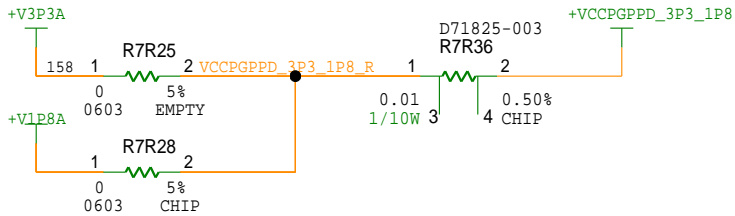
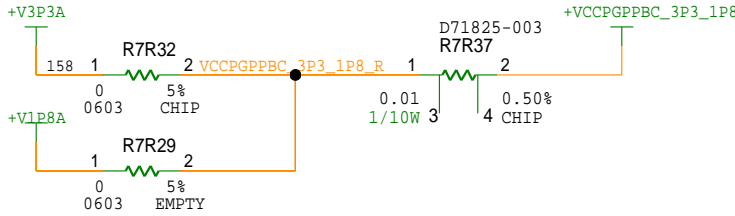
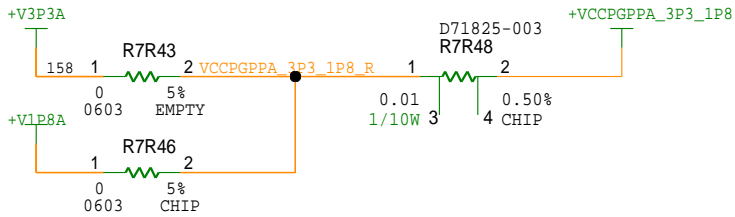
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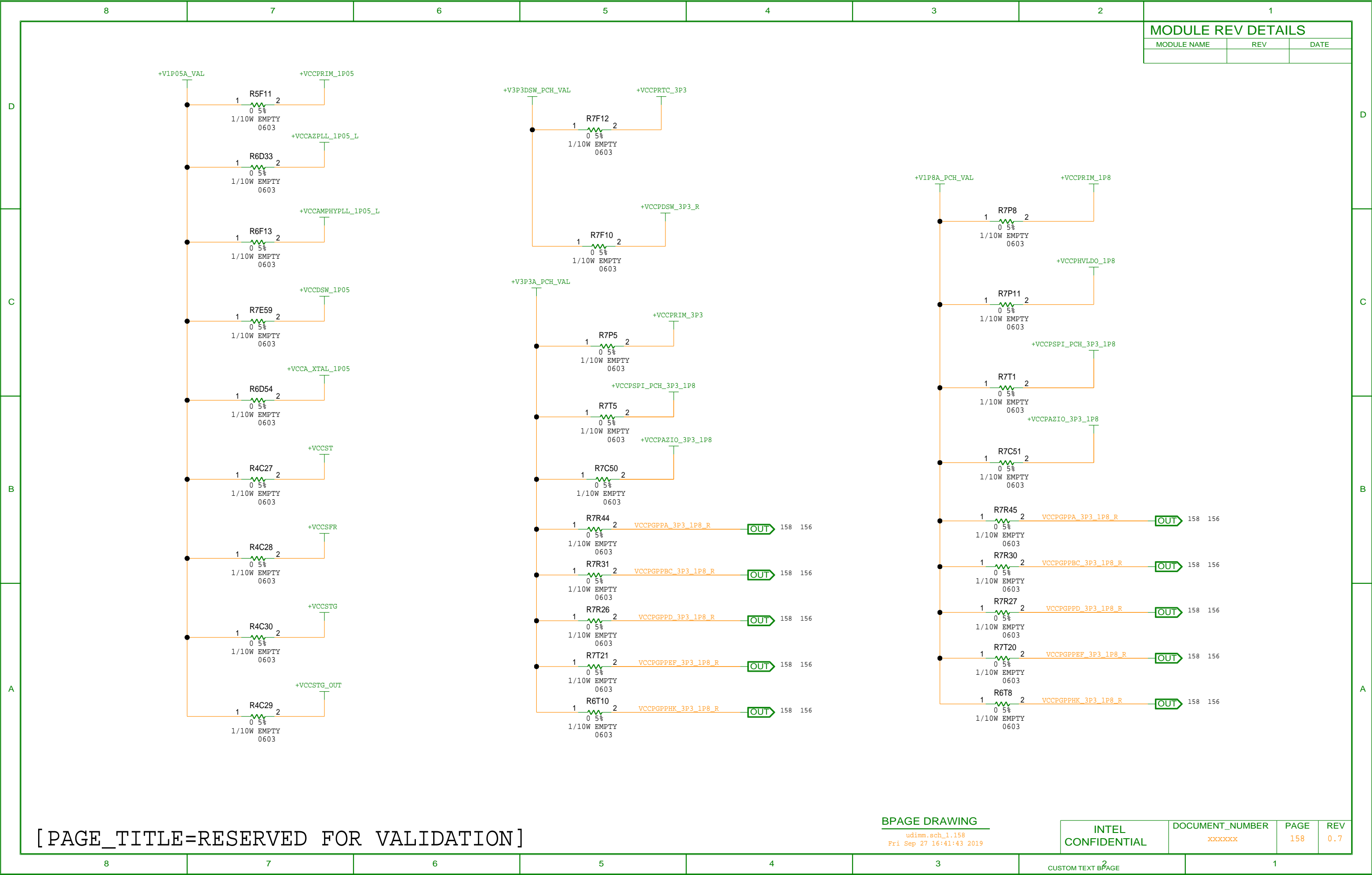
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MODULE REV DETAILS

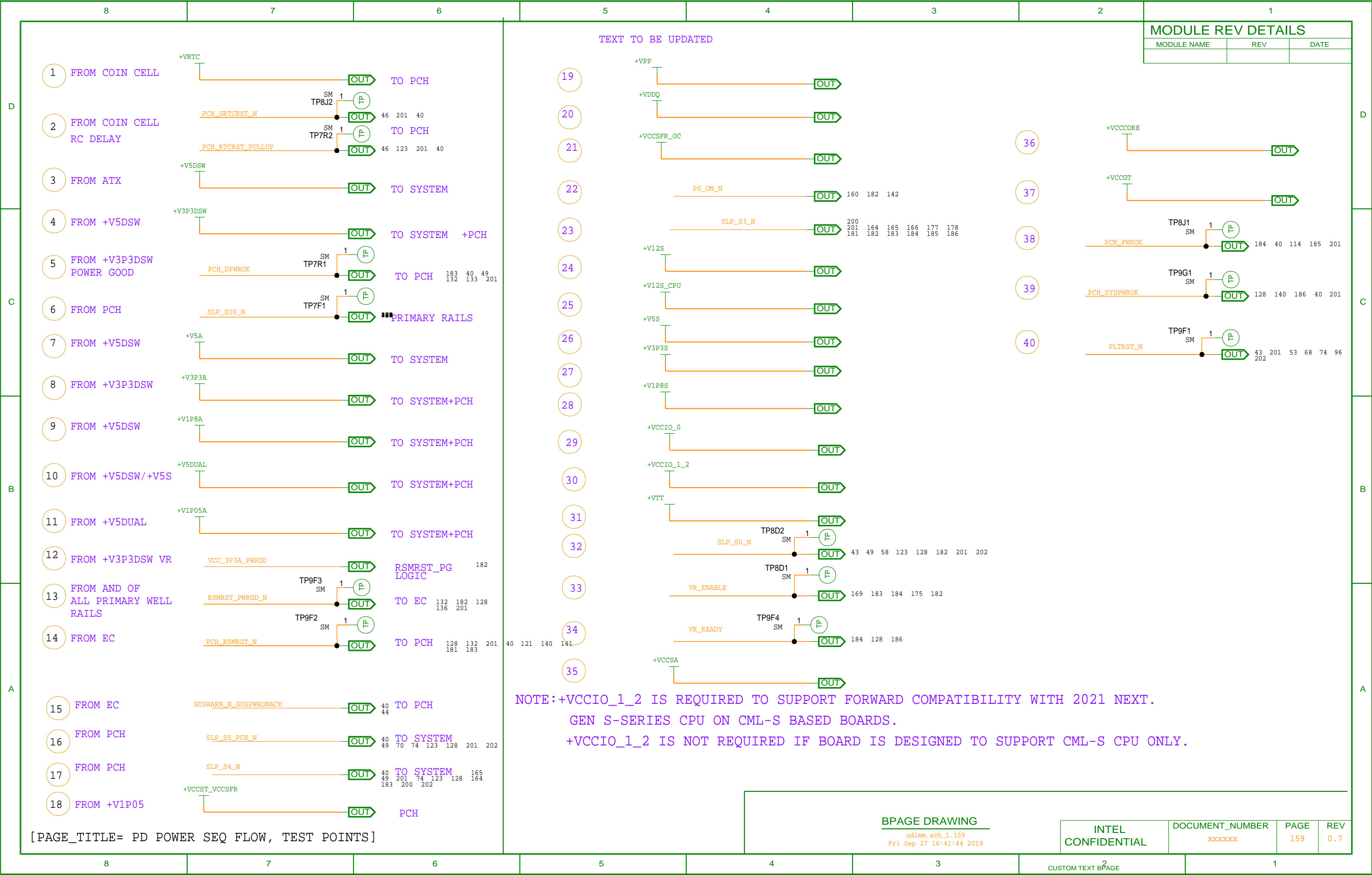
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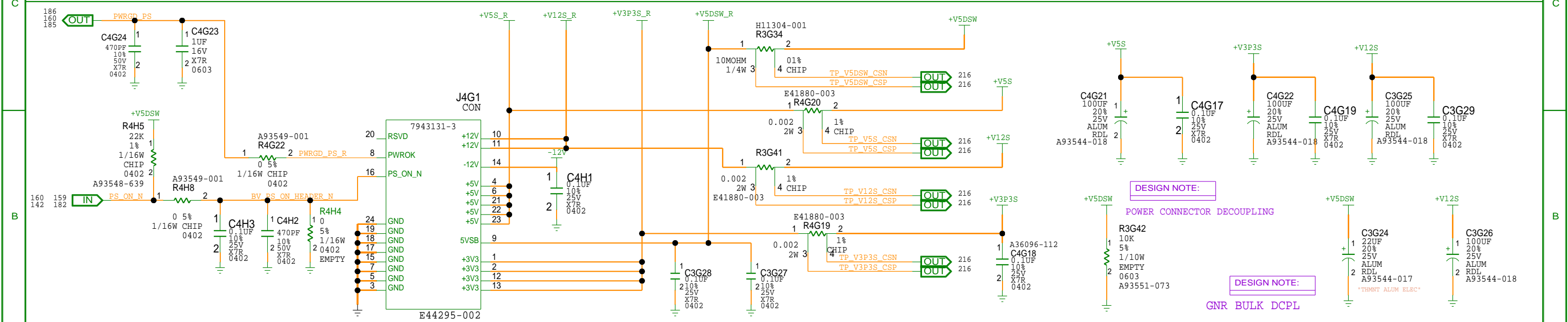


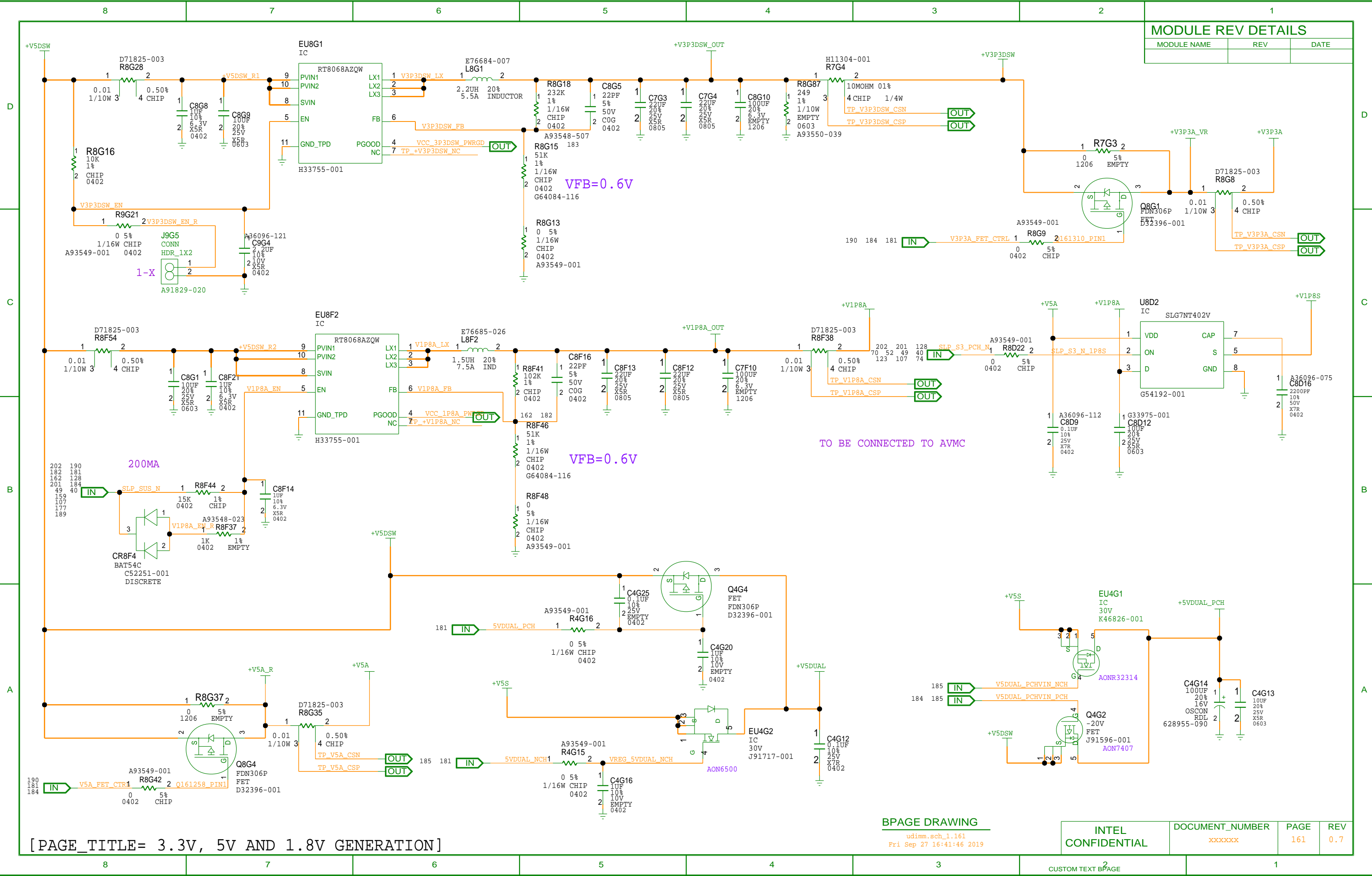










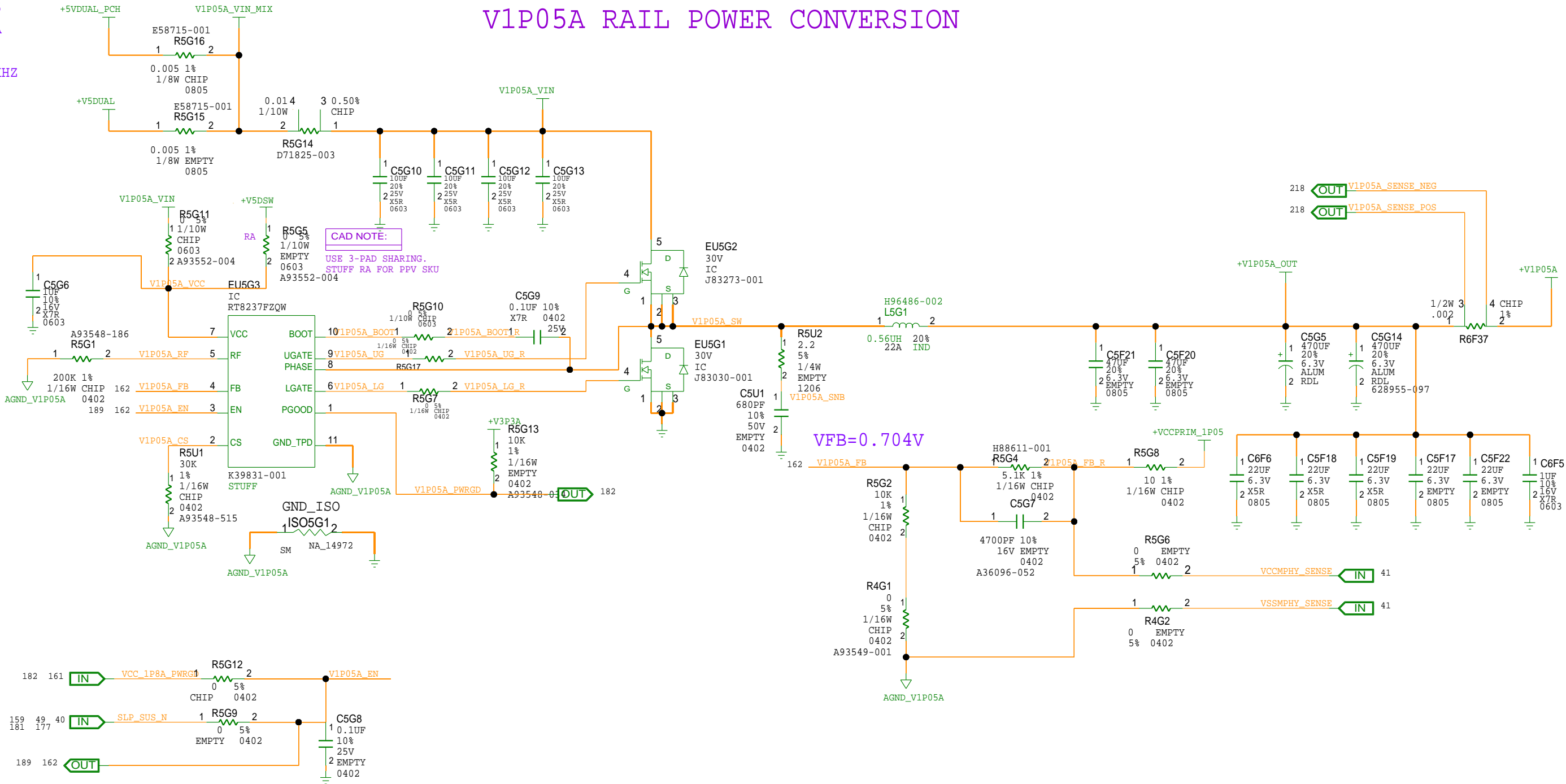


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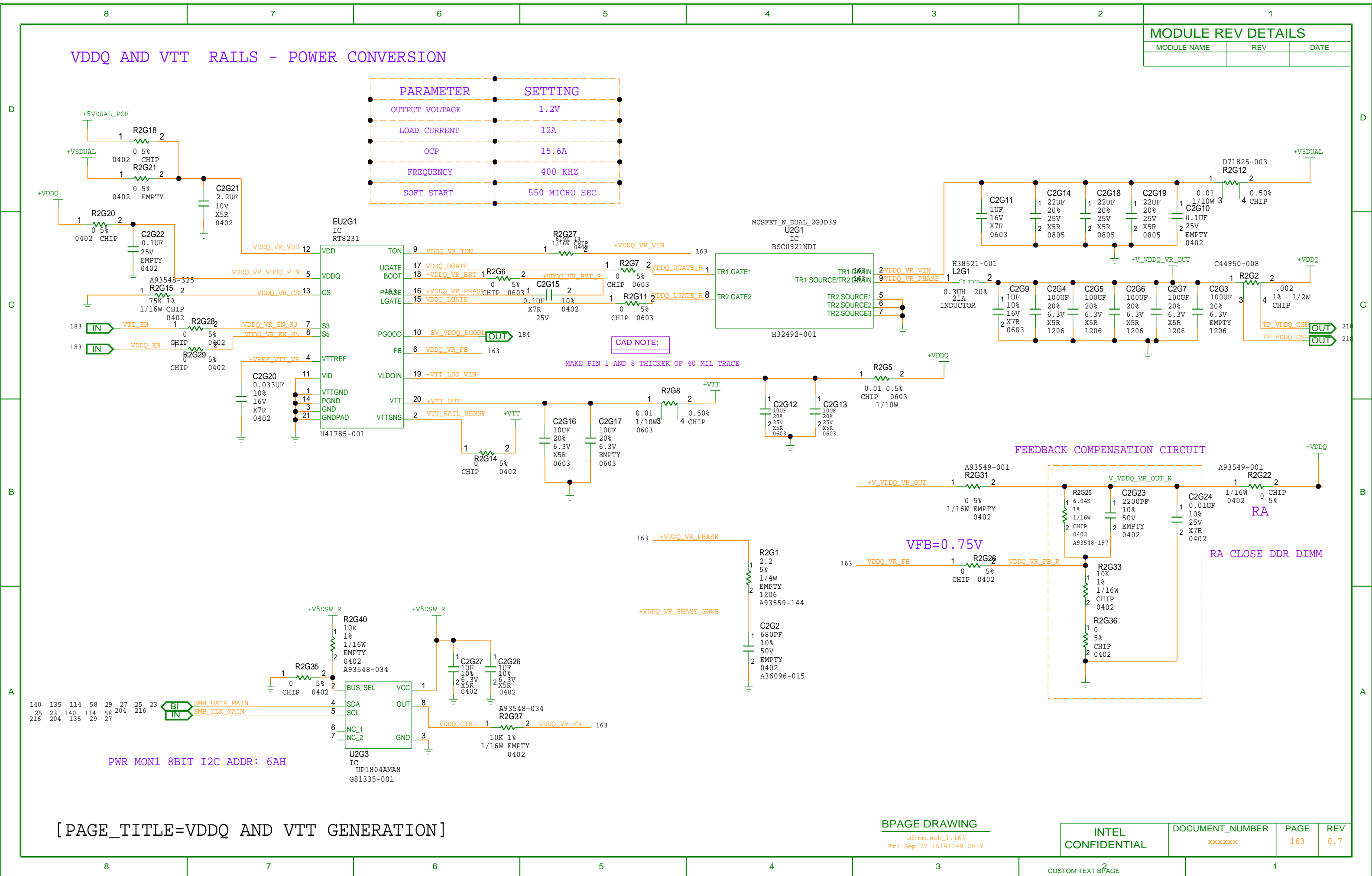
MODULE NAME	REV	DATE

RAIL : V1P05  
IOUT = 16.5A  
OCP = 20A  
SW FREQ=340KHZ

V1P05A RAIL POWER CONVERSION



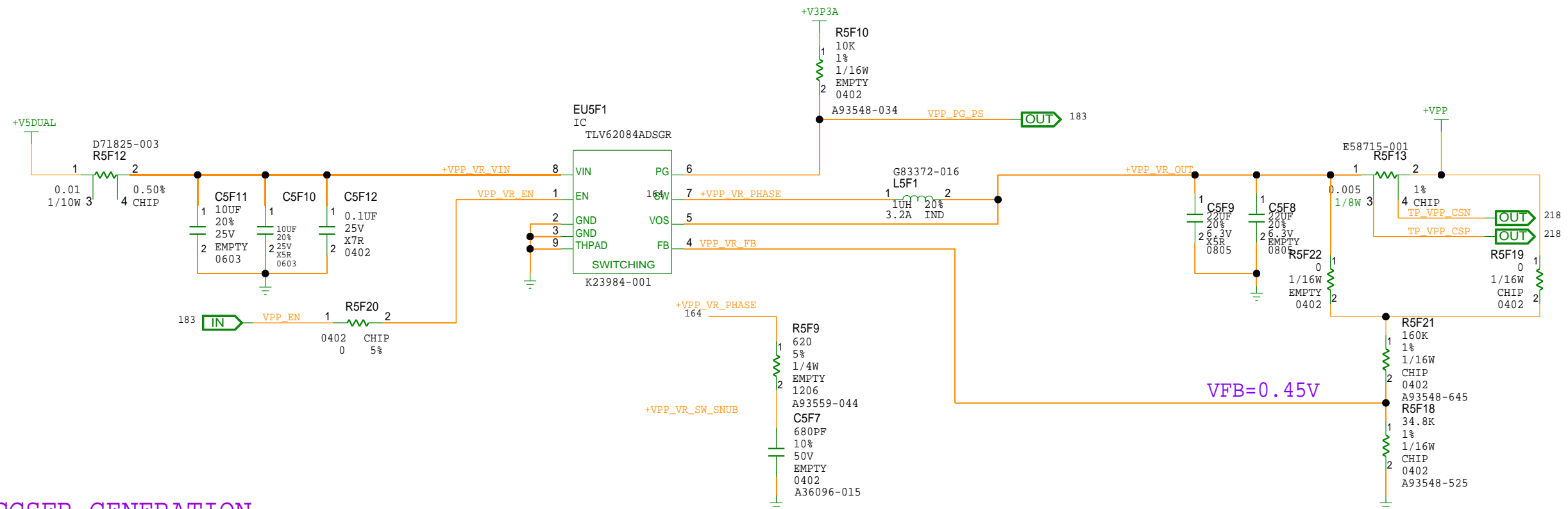
PLACE SNUBBER CLOSE TO THE FET  
PLACE C\_VCC CLOSE TO THE VR IC  
PLACE VIN CAP CLOSE TO THE CSD FET



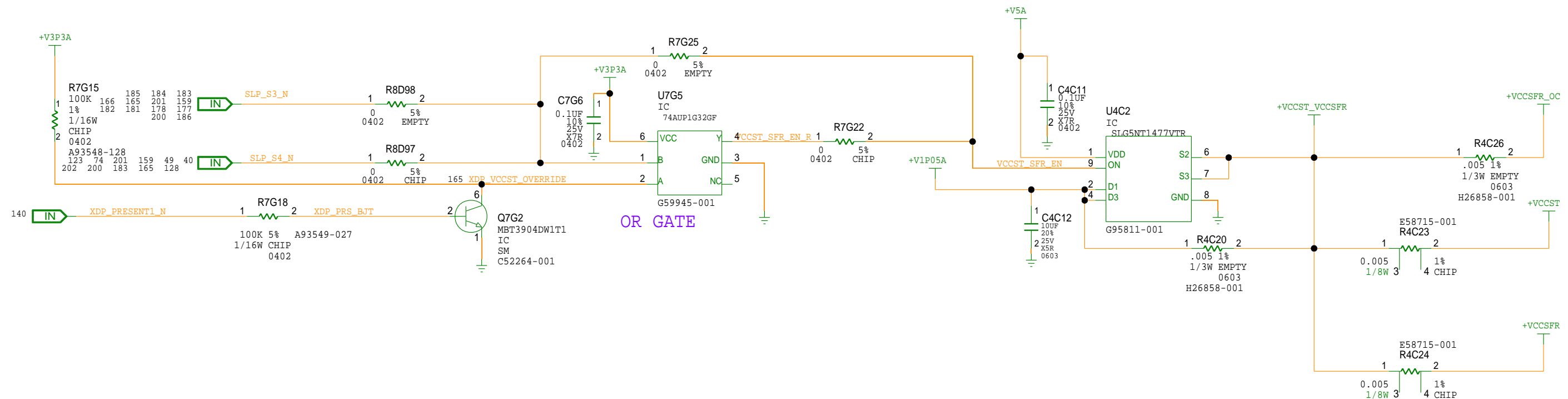
MODULE REV DETAILS		
MODULE NAME	REV	DATE

## VPP 2.5V RAIL - POWER CONVERSION

```
RAIL : 2.5V
IOOUT = 2A
OCP = 2.8A
SW FREQ=1.5MHZ
```



## VCCST & VCCSFR GENERATION



[PAGE\_TITLE=VPP &amp; VCCST\_VCCSFR GENERATION]

BPAGE DRAWING

udimm.sch\_1.164  
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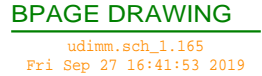
CUSTOM TEXT B<sup>2</sup>PAGE

1



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## [ PAGE\_TITLE=VCCSTG



## D

SW FREQ=1.5MHZ



## B



REV

1

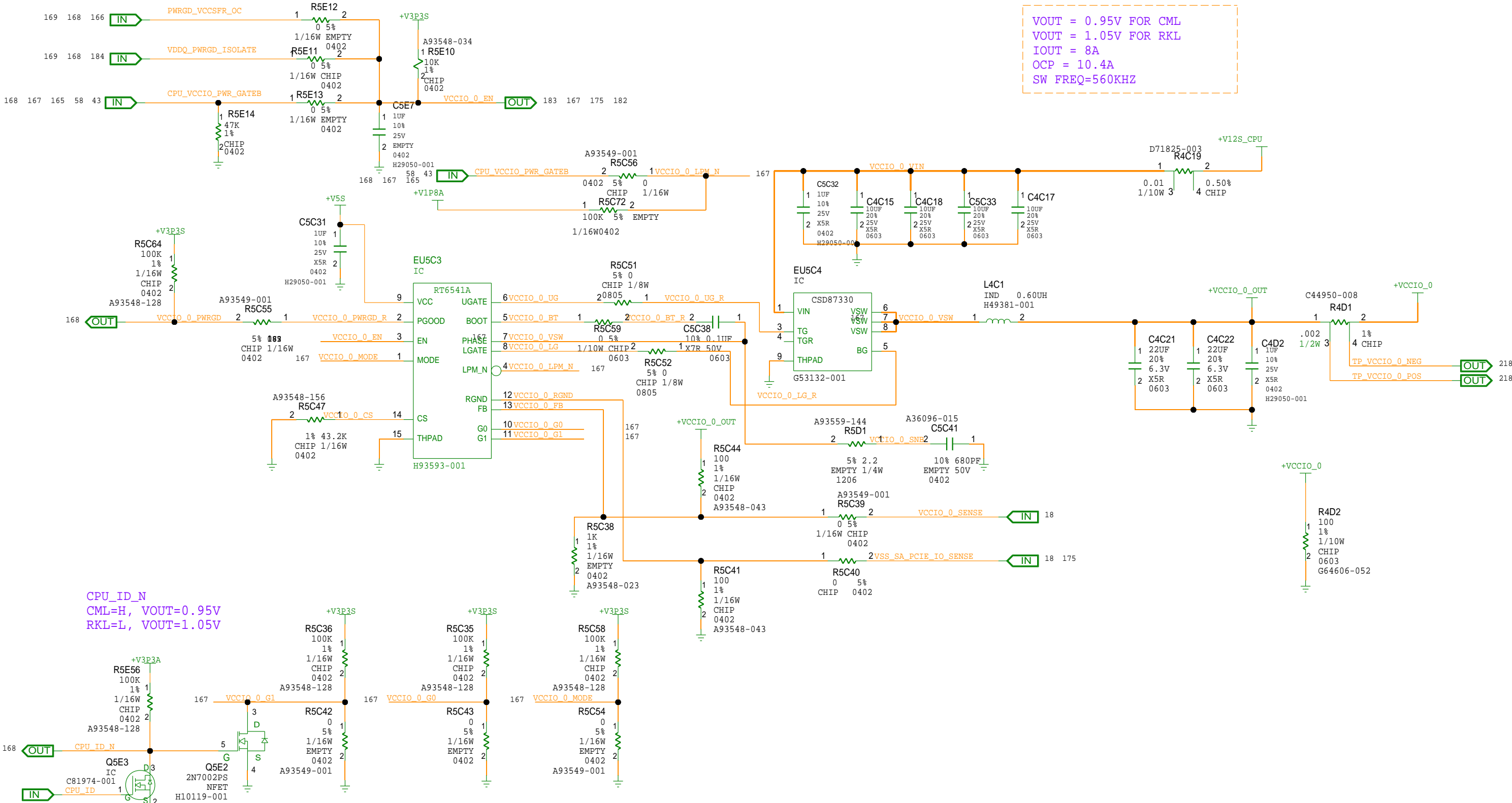


MODULE REV DETAILS

MODULE NAME	REV	DATE

VCCIO\_0

VOUT = 0.95V FOR CML  
VOUT = 1.05V FOR RKL  
IOUT = 8A  
OCP = 10.4A  
SW FREQ=560KHZ



[PAGE\_TITLE=VCCIO\_0 GENERATION]

BPAGE DRAWING

udimm.sch\_1.167  
Fri Sep 27 16:41:55 2019

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DOCUMENT\_NUMBER

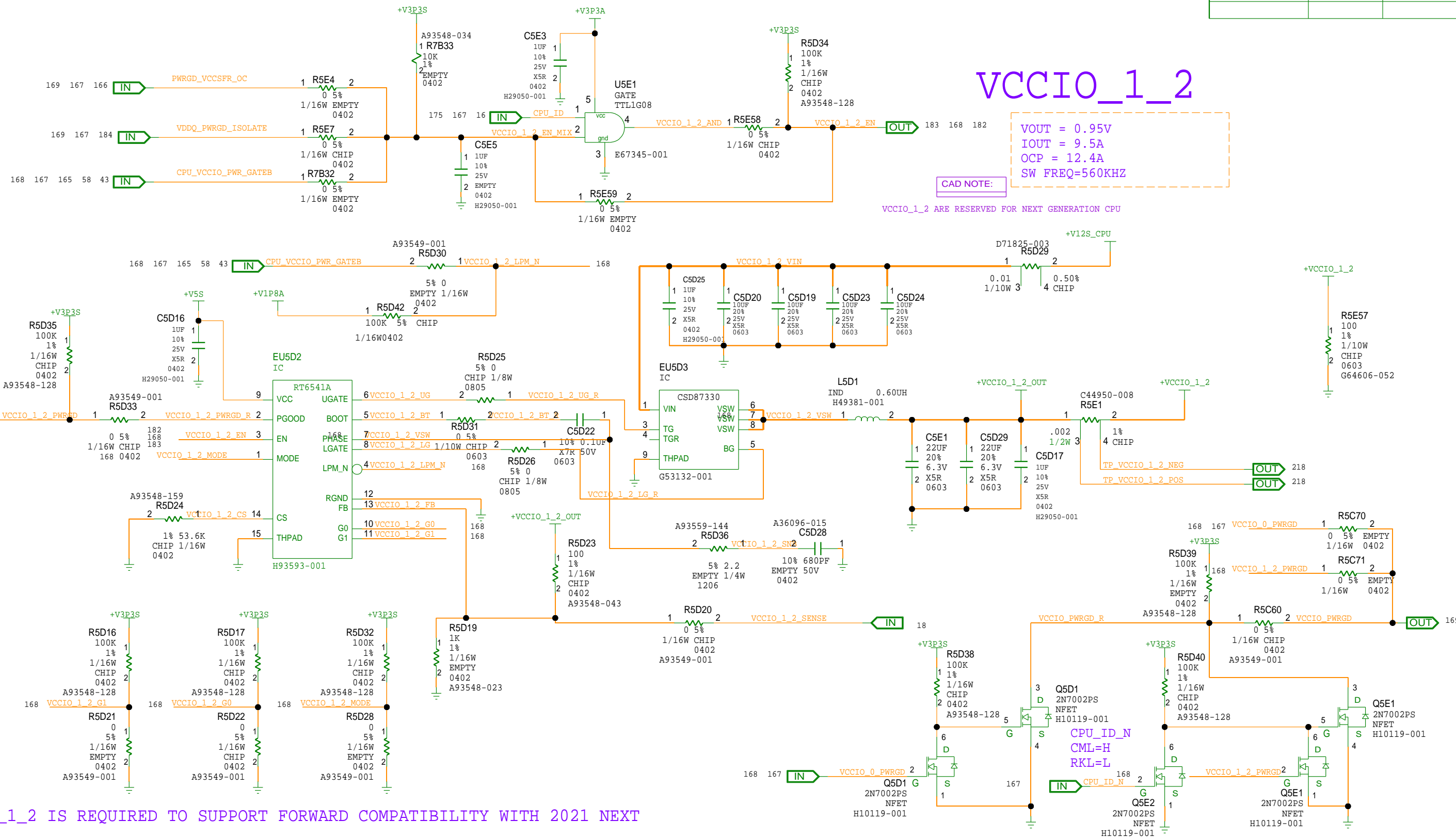
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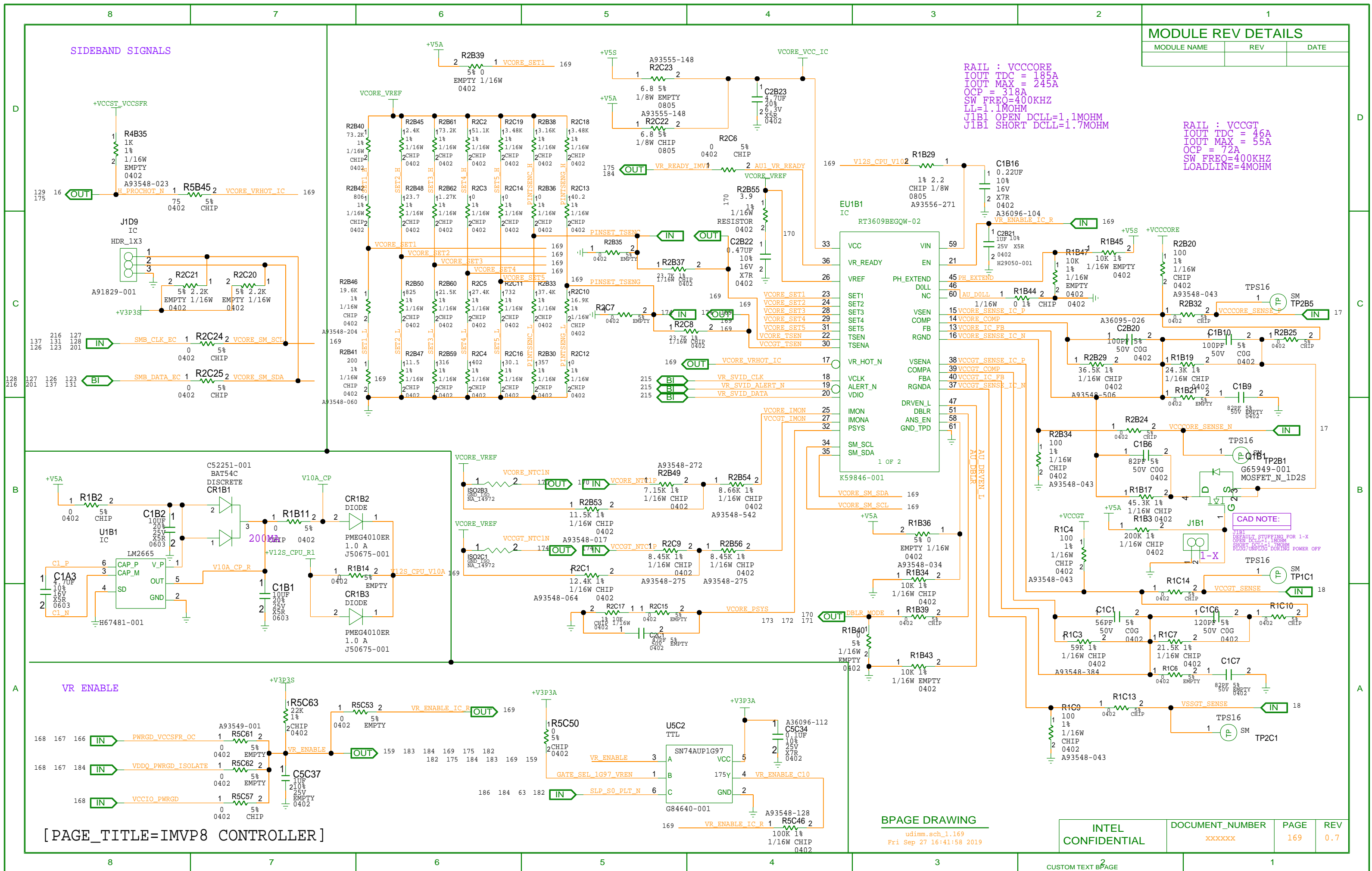
167

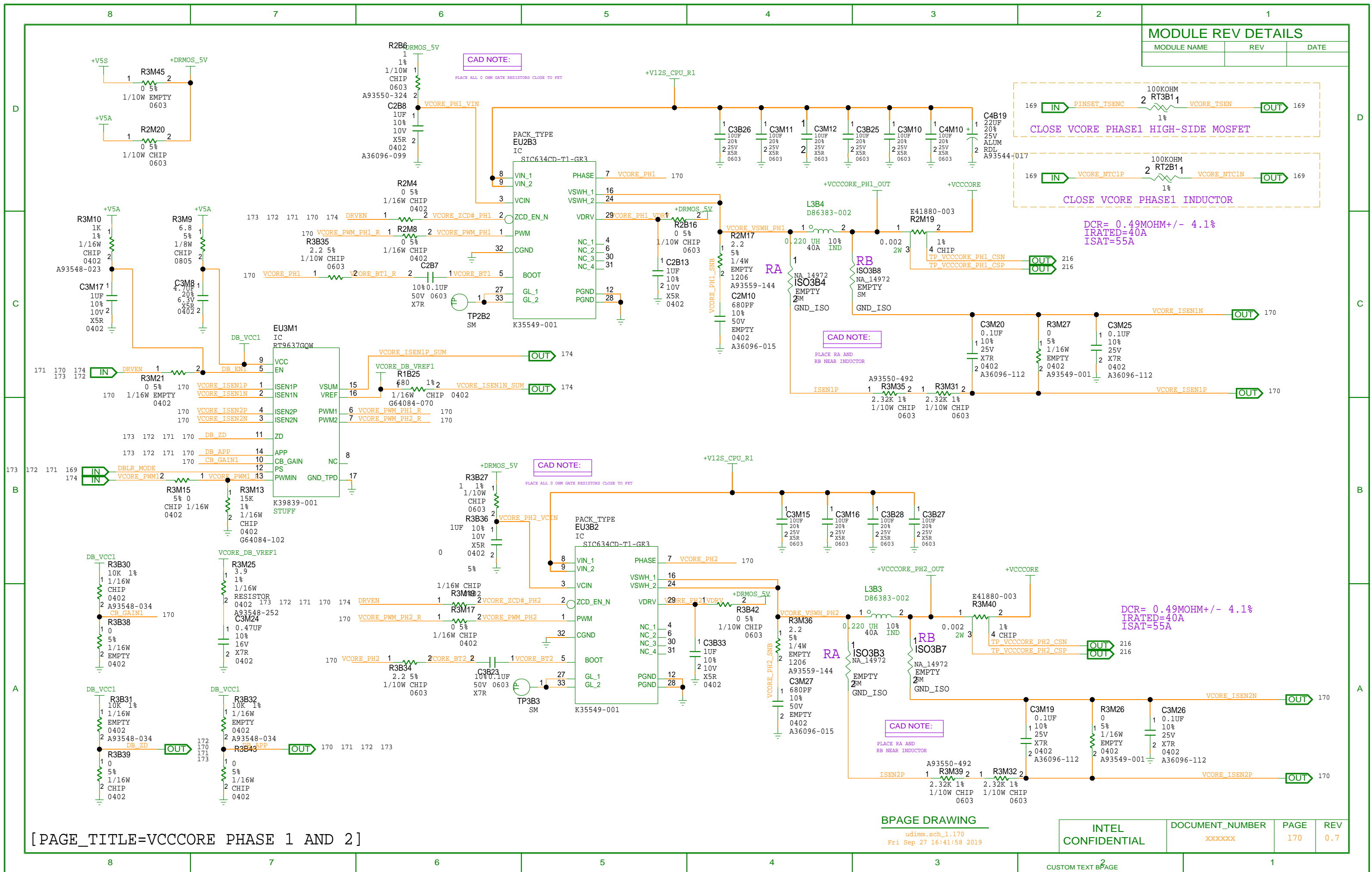
REV

0.7

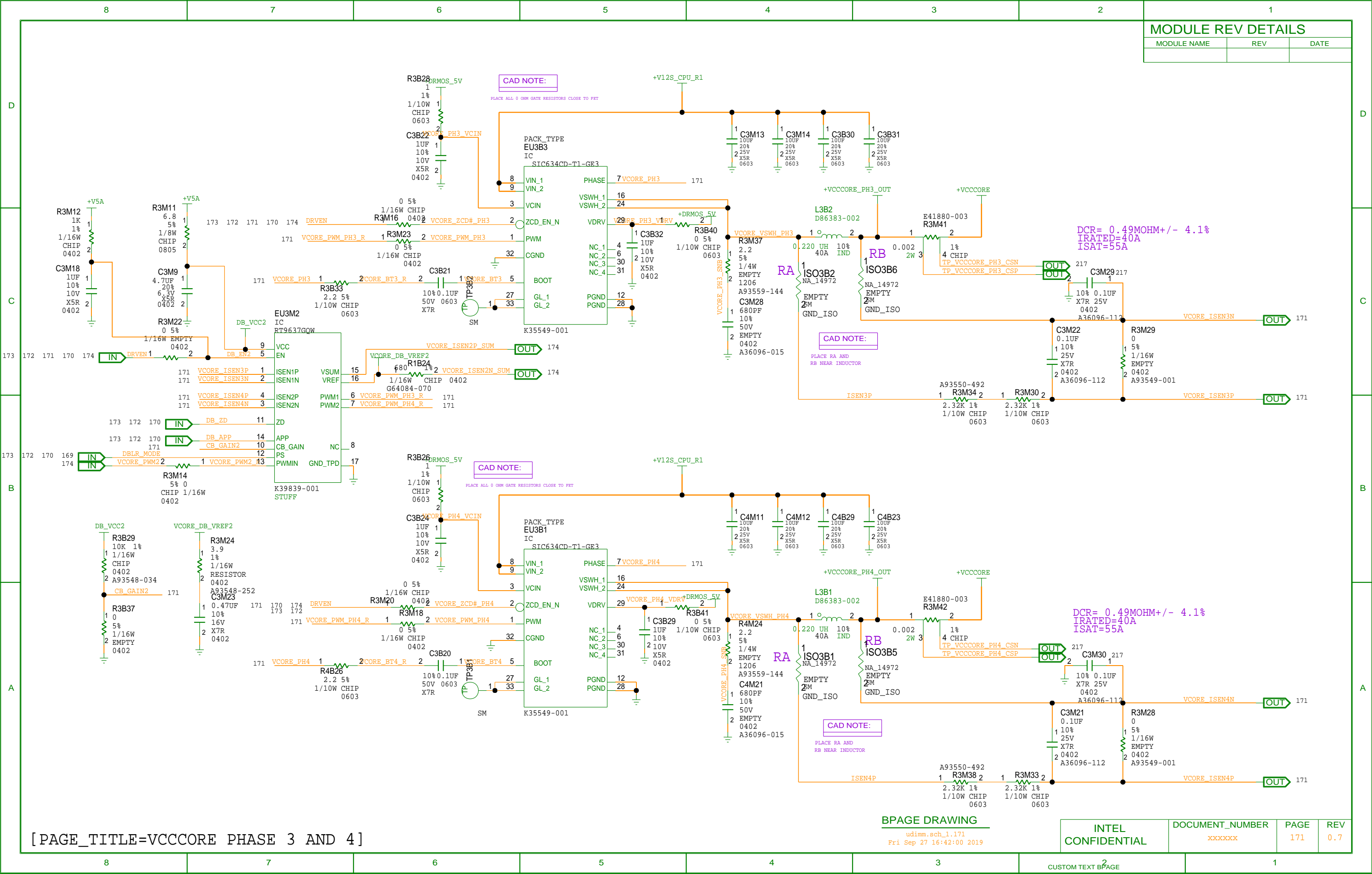


NOTE:+VCCIO\_1\_2 IS REQUIRED TO SUPPORT FORWARD COMPATIBILITY WITH 2021 NEXT  
GEN S-SERIES CPU ON CML-S BASED BOARDS.  
+VCCIO\_1\_2 IS NOT REQUIRED IF BOARD IS DESIGNED TO SUPPORT CML-S CPU ONLY.









[ PAGE\_TITLE=VCCCORE PHASE 3 AND 4 ]

MODULE REV DETAILS

MODULE NAME	REV	DATE

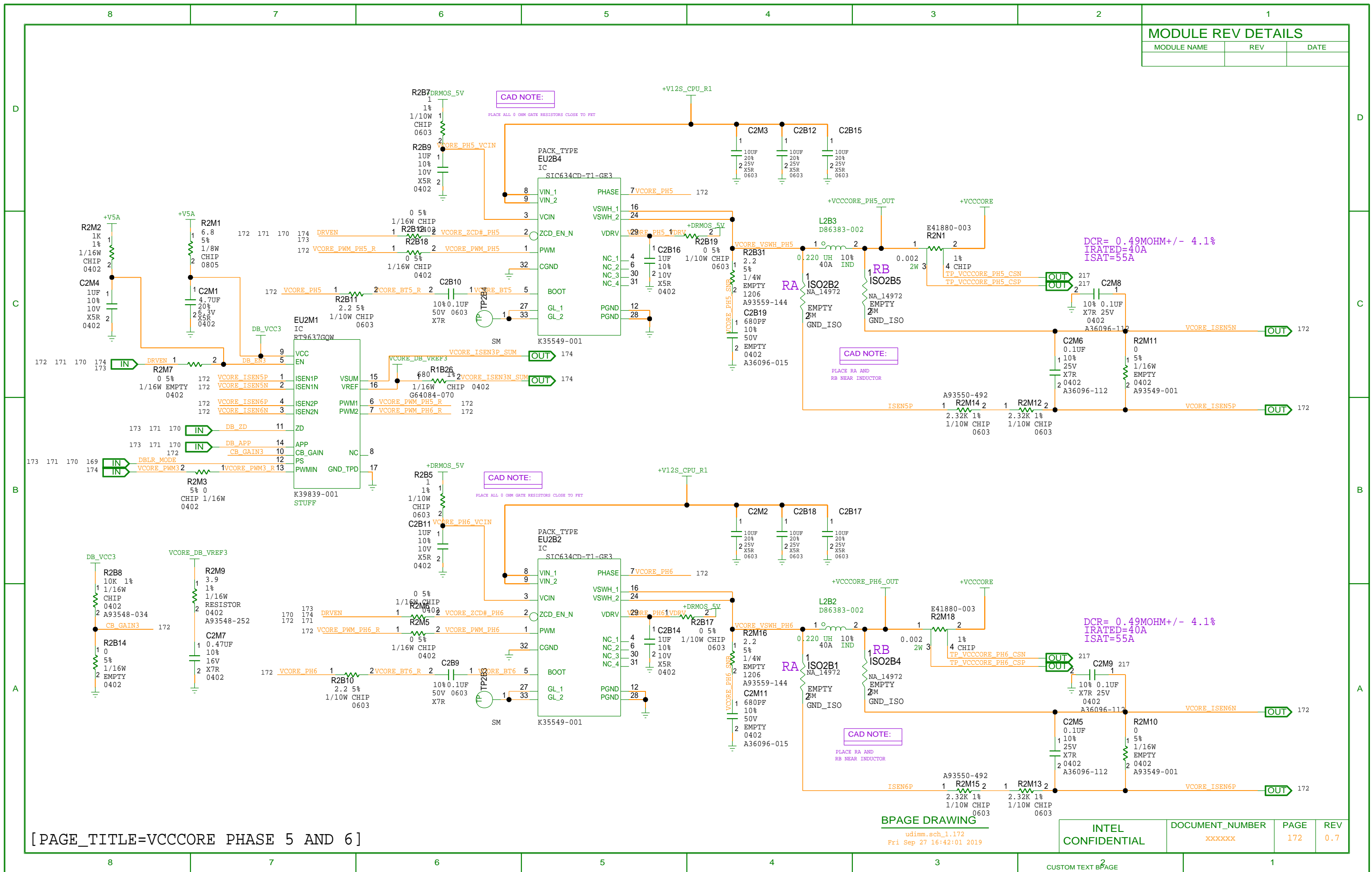
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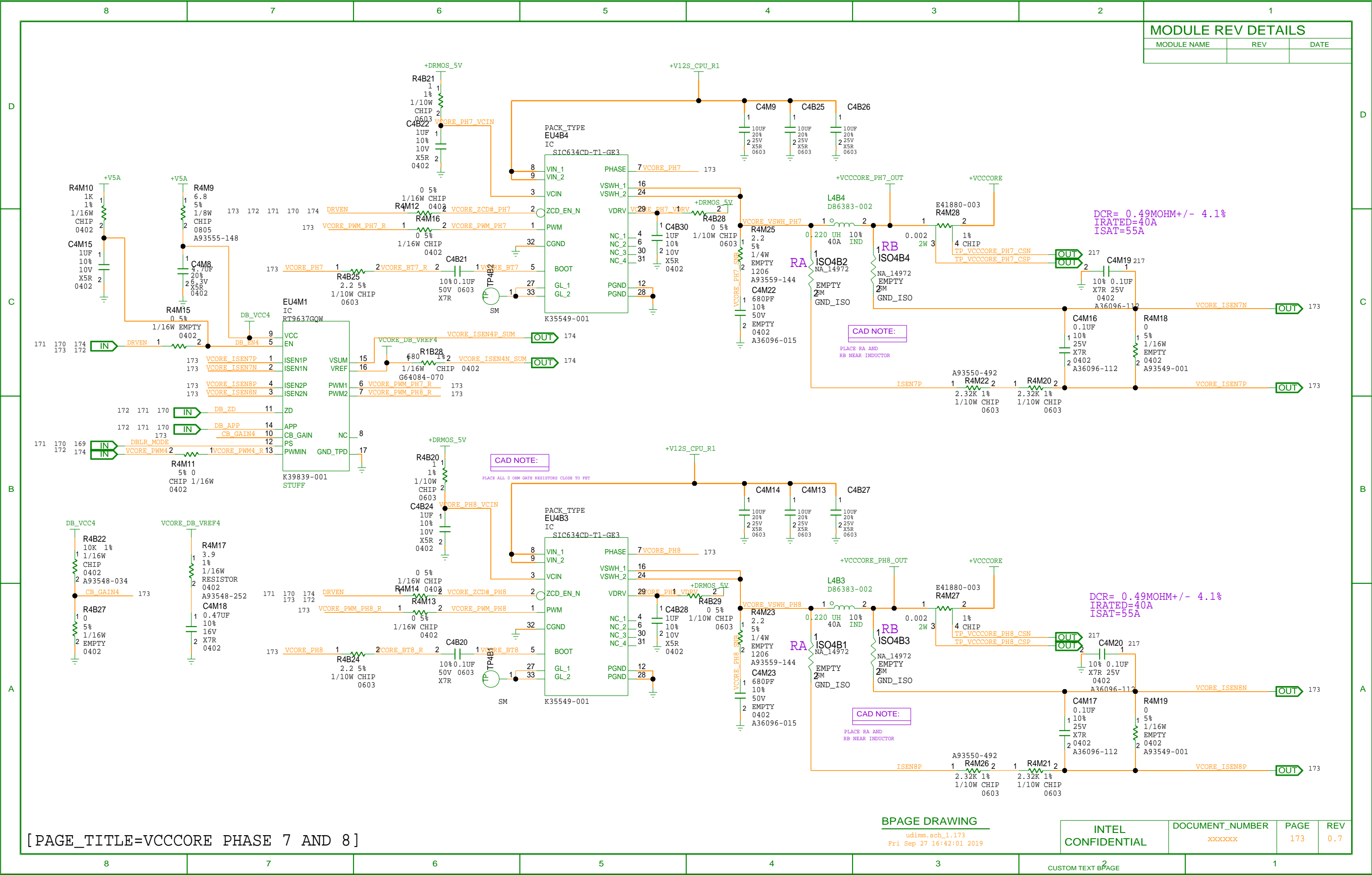
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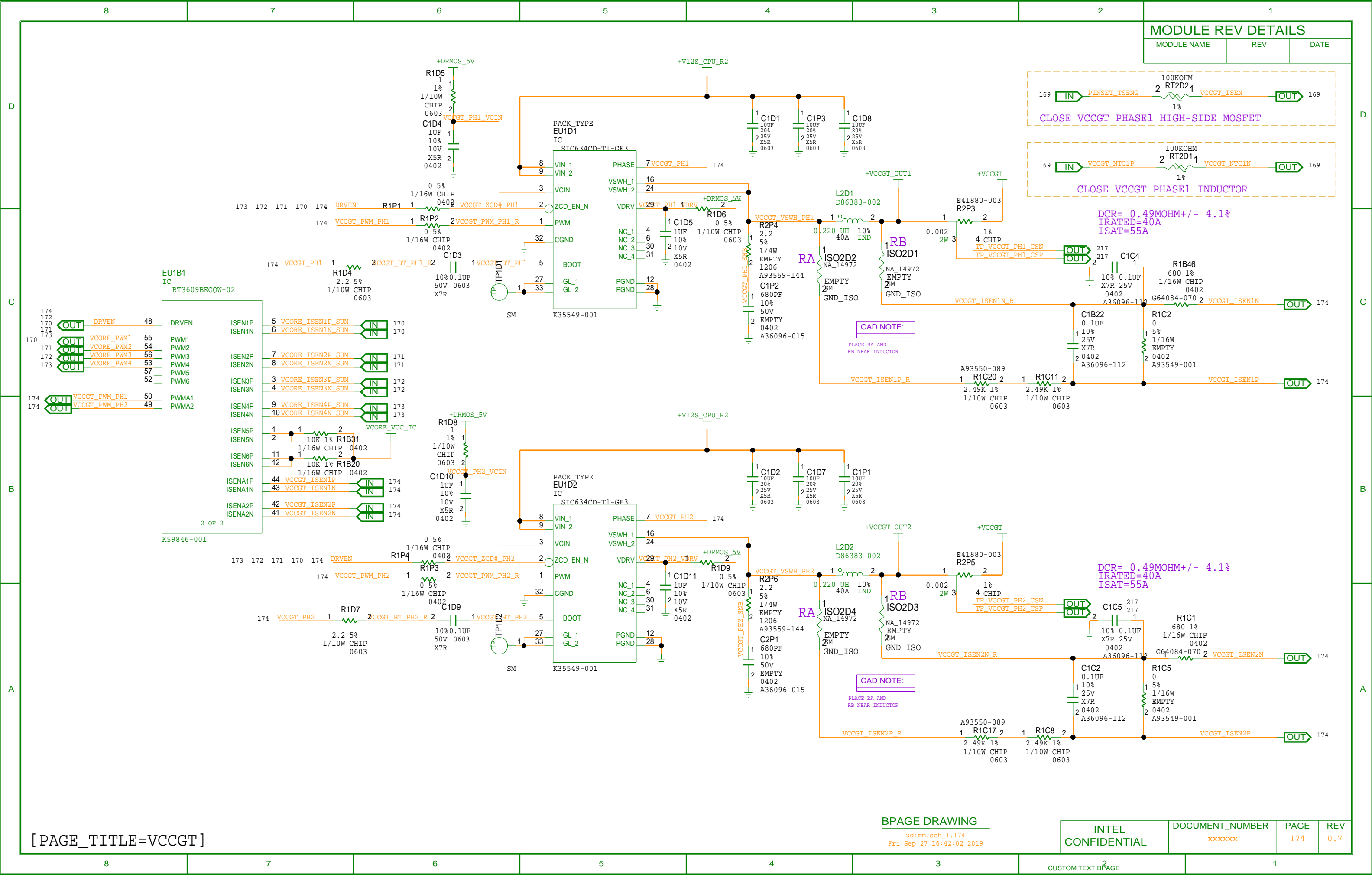
PAGE  
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0.7

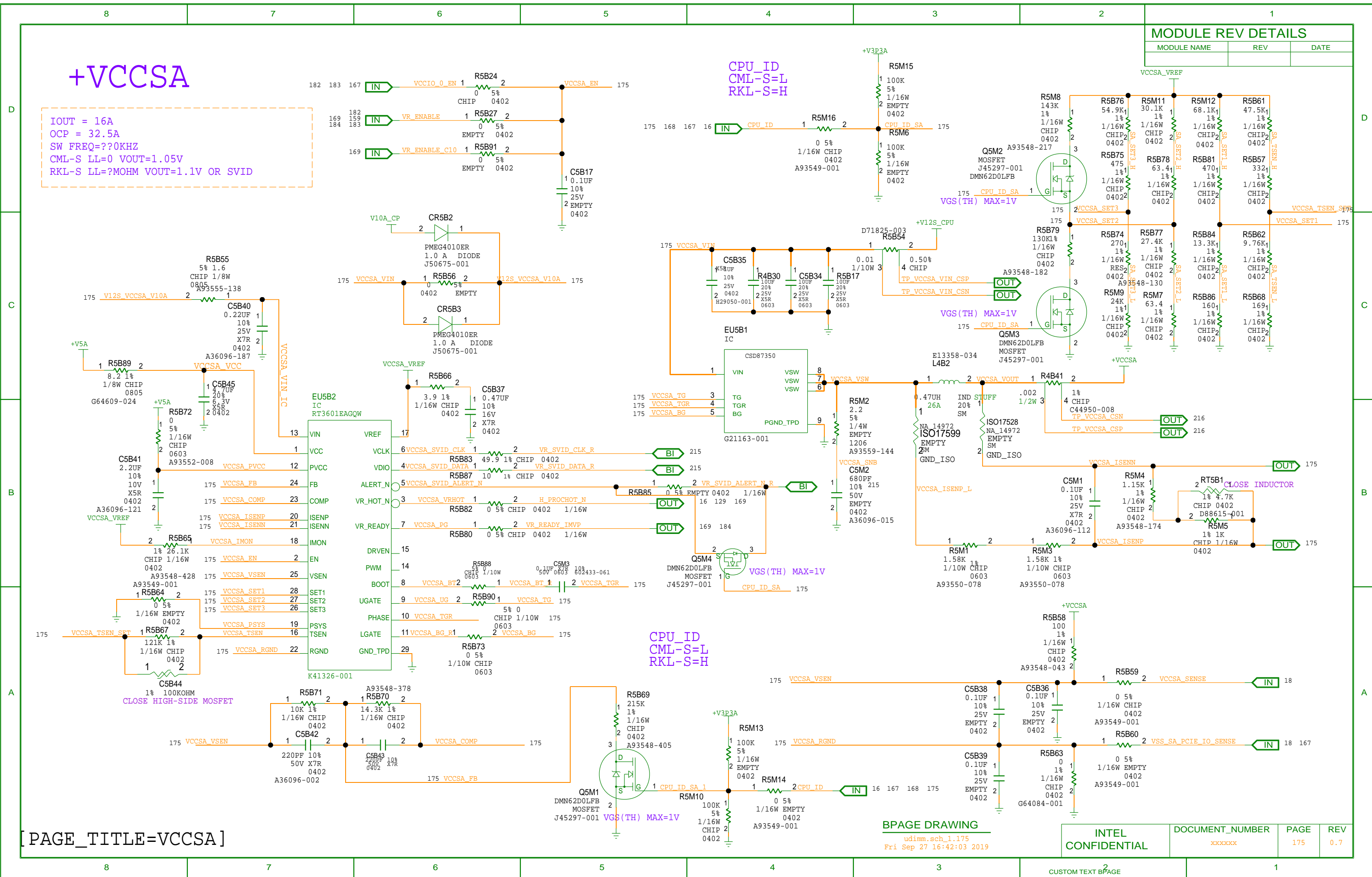
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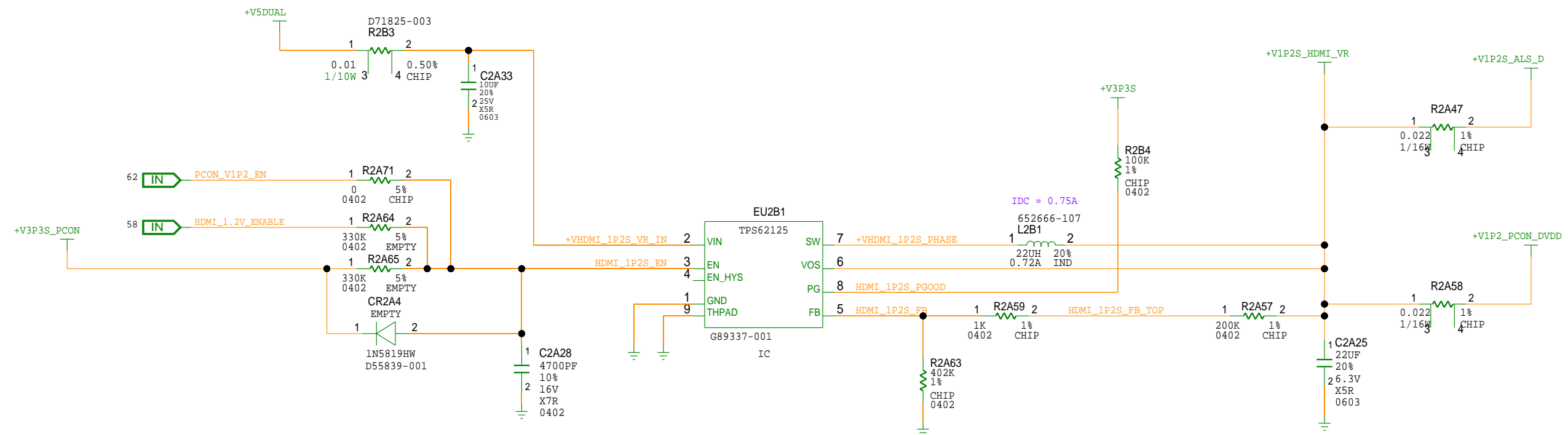




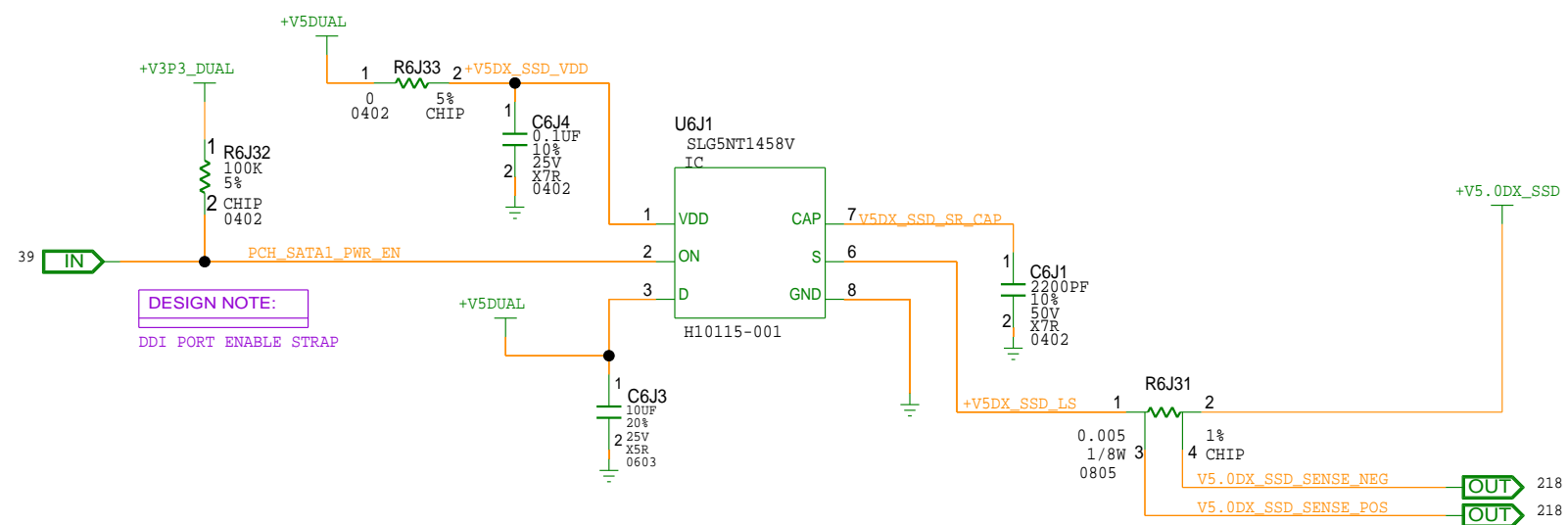
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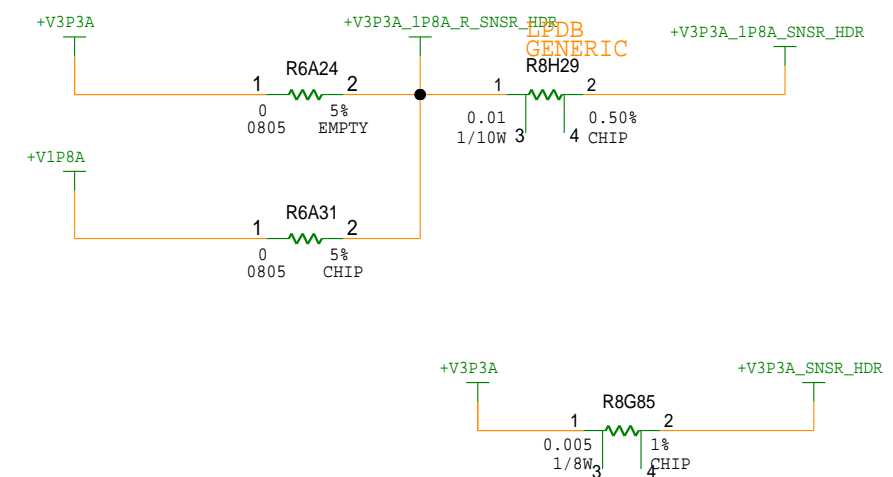
## 1P2V RAIL FOR HDMI AND UFS - POWER CONVERSION



## V5DX\_SSD DIRECT CONNECT GENERATION



## ISH AIC POWER GENERATION



BPAGE DRAWING

udimm.sch\_1.176  
Fri Sep 27 16:42:04 2019

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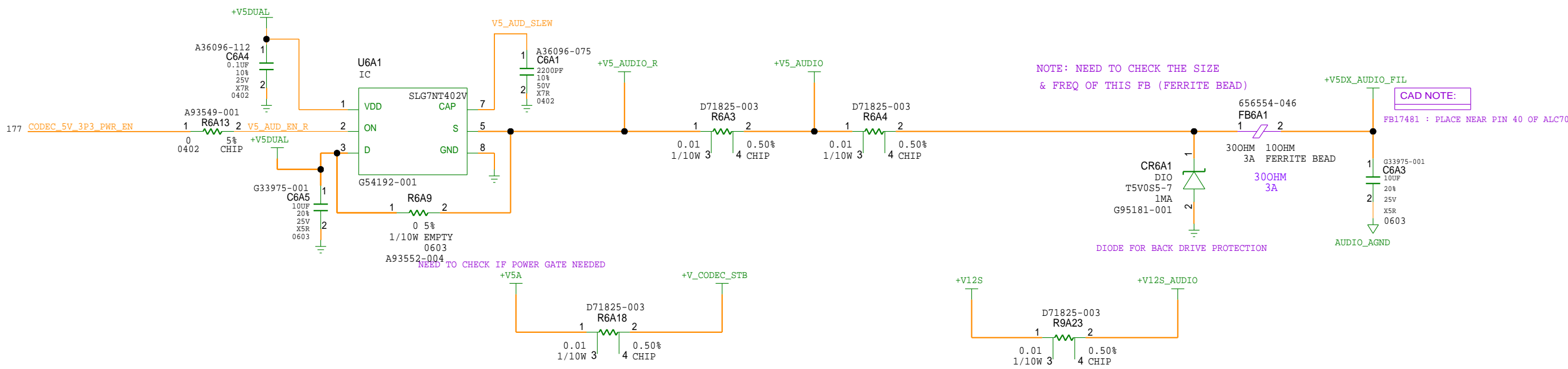
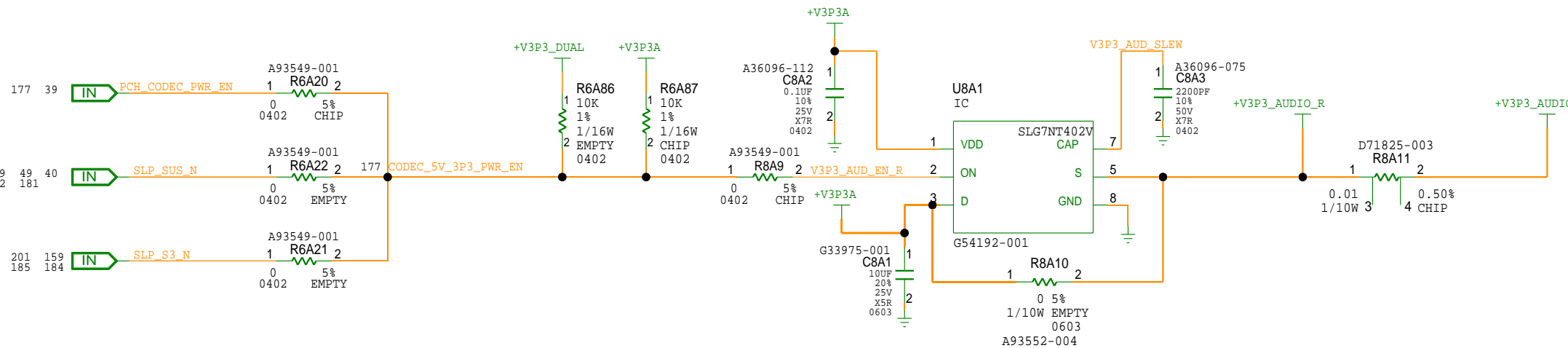
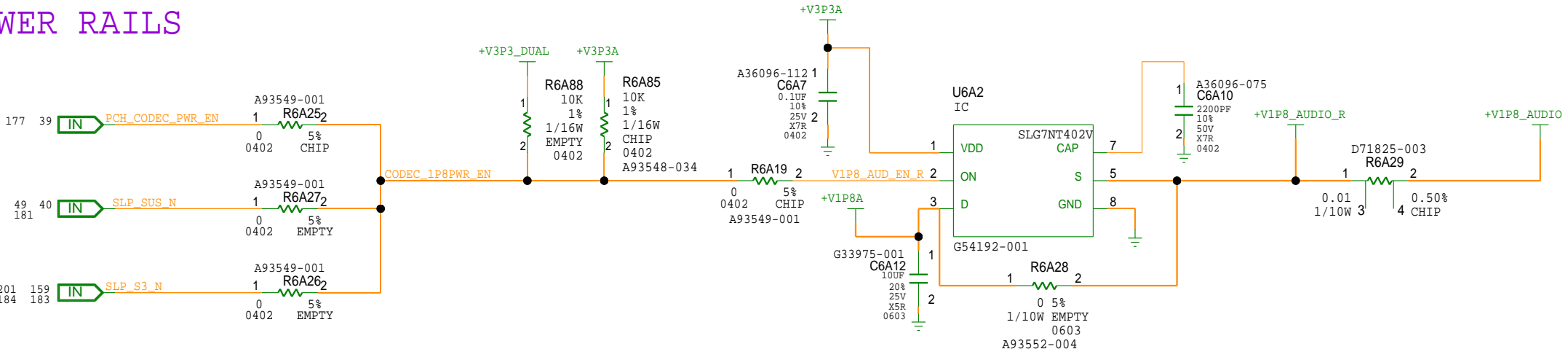
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[PAGE\_TITLE= 1P2V FOR HDMI AND SSD AND ISH RAILS

AUDIO POWER RAILS

MODULE REV DETAILS

MODULE NAME	REV	DATE



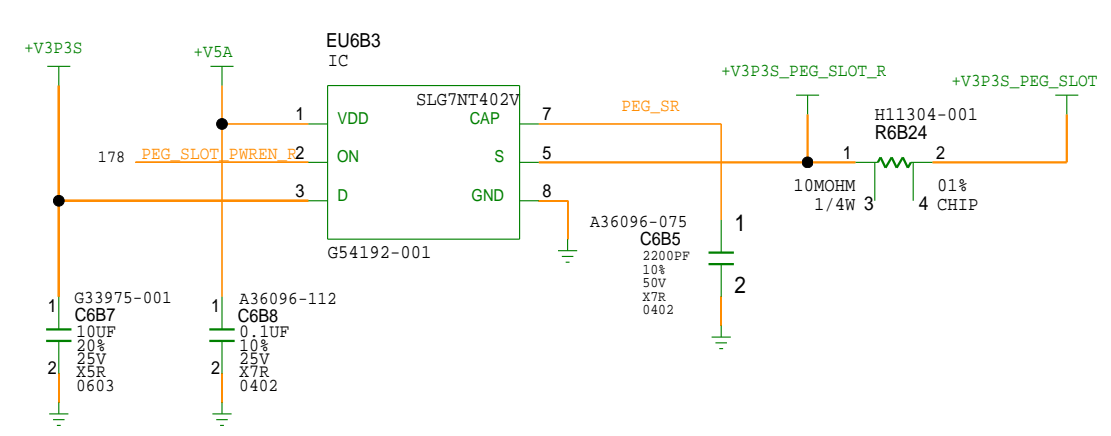
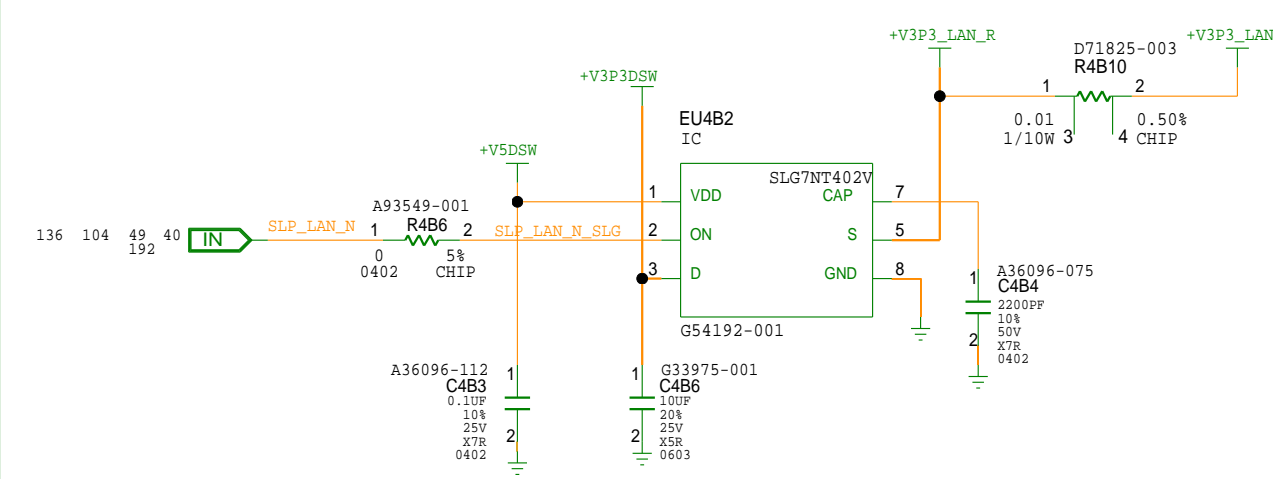
NOTE: NEED TO CHECK THE SIZE & FREQ OF THIS FB (FERRITE BEAD)

CAD NOTE:

FB17481 : PLACE NEAR PIN 40 OF ALC700

NEED TO CHECK IF POWER GATE NEEDED

DIODE FOR BACK DRIVE PROTECTION



BPAGE DRAWING

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udimm.sch\_1.178  
Fri Sep 27 16:42:06 2019

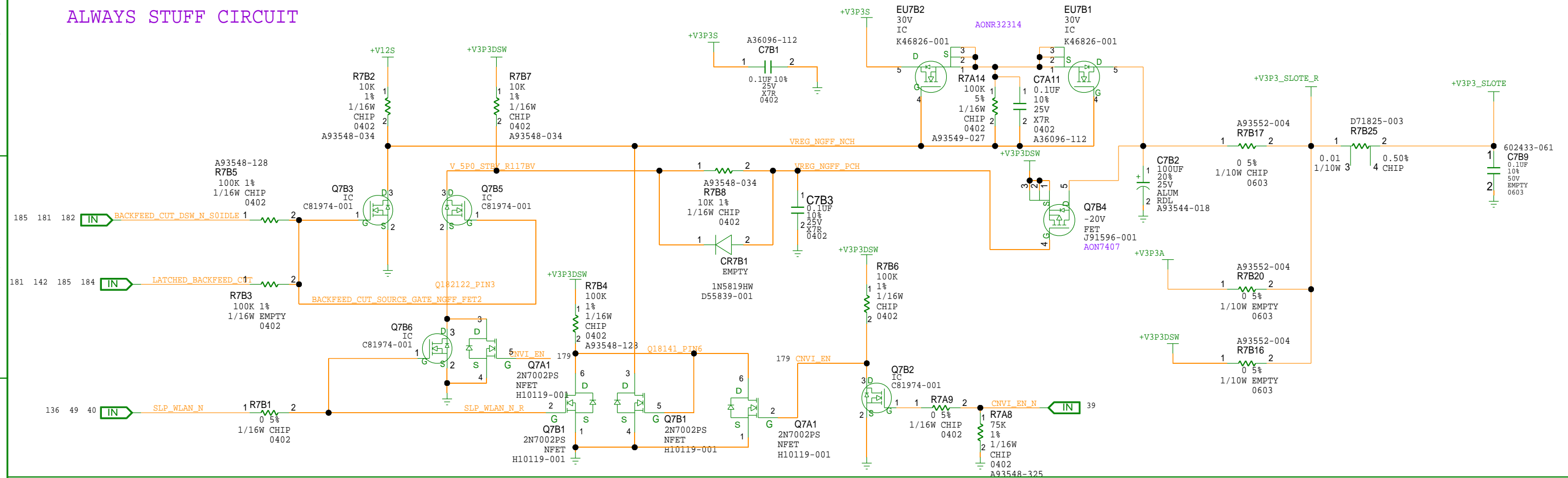
INTEL CONFIDENTIAL	DOCUMENT_NUMBER xxxxxxx	PAGE 178	REV 0.7
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## MODULE REV DETAILS

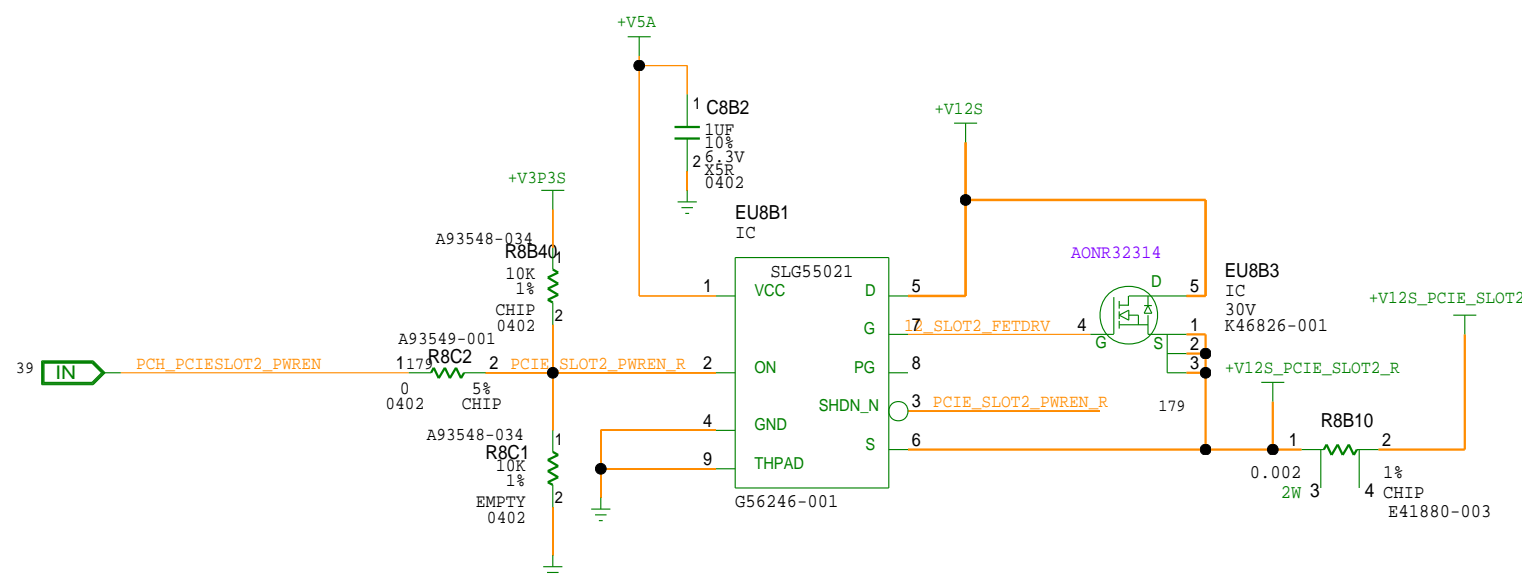
MODULE NAME	REV	DATE

**DESIGN NOTE:**

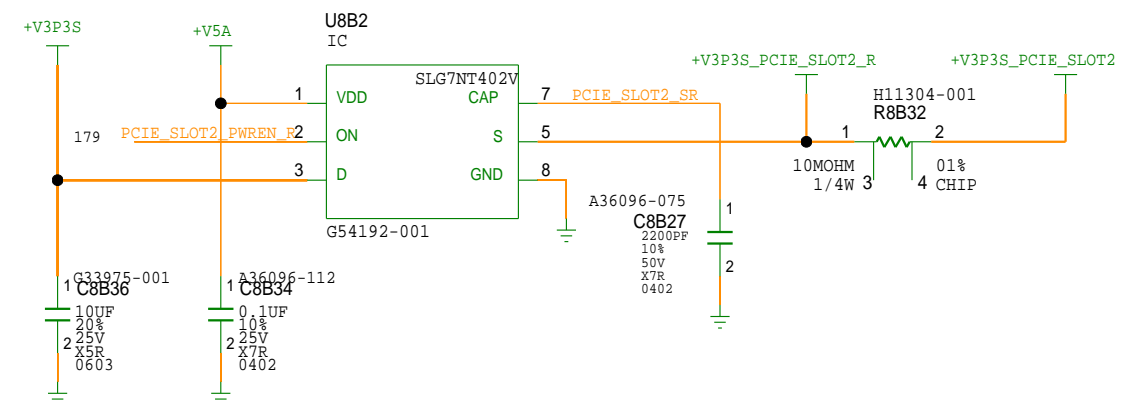
### 3.3 NGFF WIRELESS LAN SWITCH LOGIC ALWAYS STUFF CIRCUIT



## V12S PCIE SLOT2 GENERATION



## V3P3S PCIE SLOT2 GENERATION



[PAGE\_TITLE=3P3 NGFF WIRELESS AND PCIE SLOT2 POWER]

BPAGE DRAWING

udimm.sch\_1.179  
Fri Sep 27 16:42:07 2019

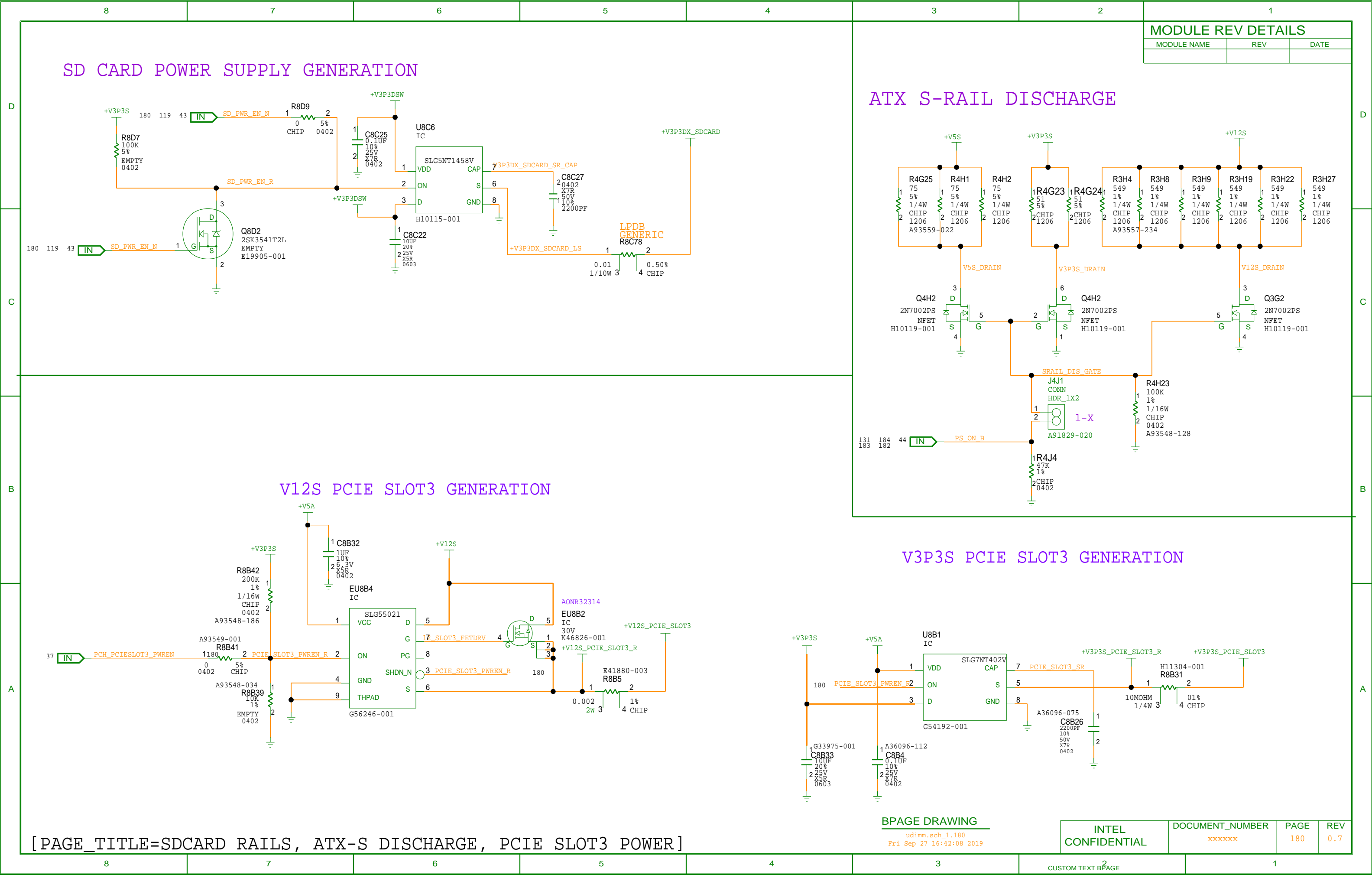
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DOCUMENT_NUMBER	XXXXXX
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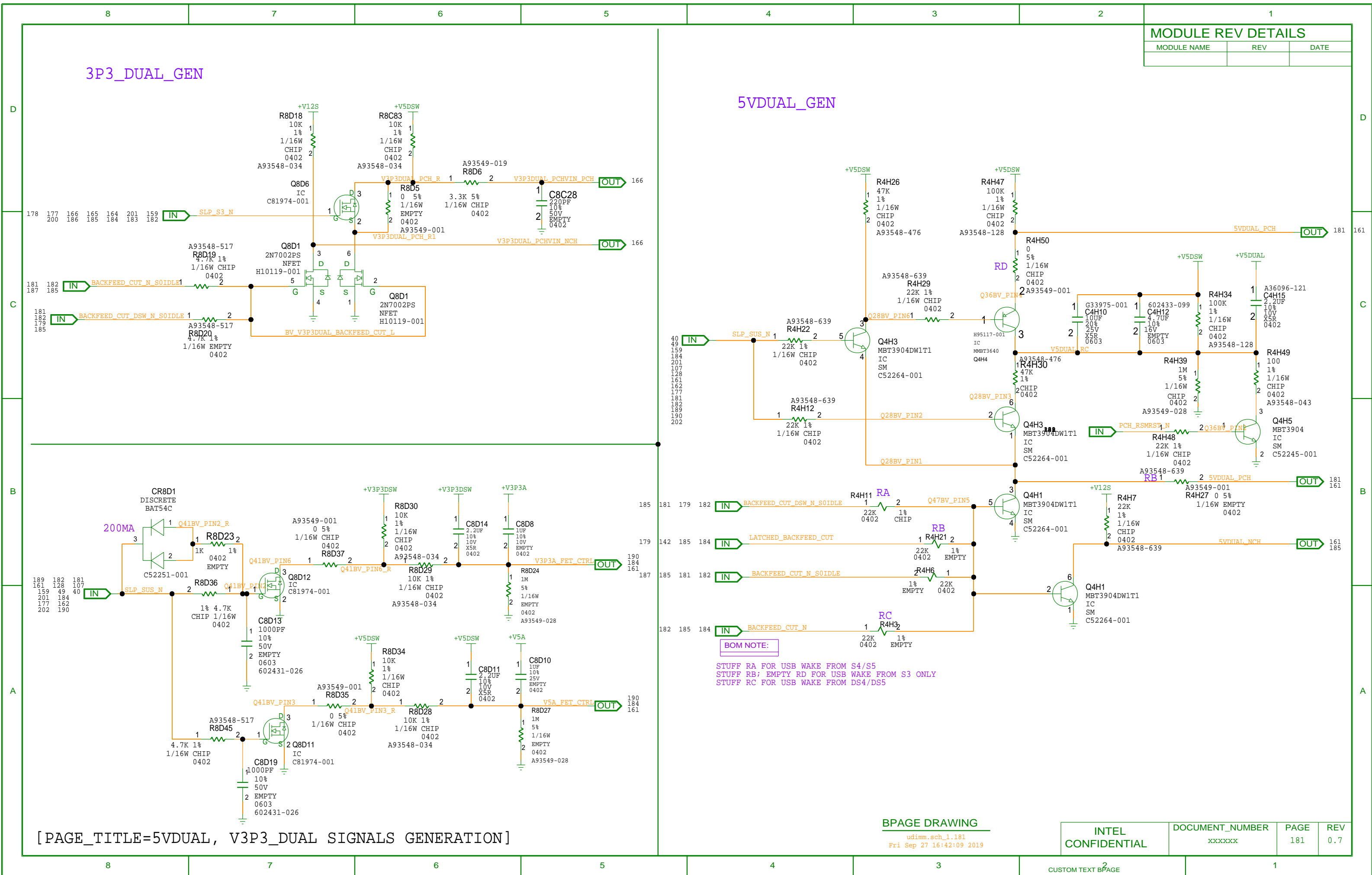
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## PS ON LOGIC



## C



## A



## REQUEST EC TO GENERATE 10MS DELAY

## CEC RELATED SEQ LOGIC



OR GATE WITH  
INPUT C INVERTED

OR GATE WITH  
INPUT C INVERTED

7 OR GATE WITH  
INPUT C INVERTED

## QUICK RSMRST\_N PULL DN CKT

## BPAGE DRAWING

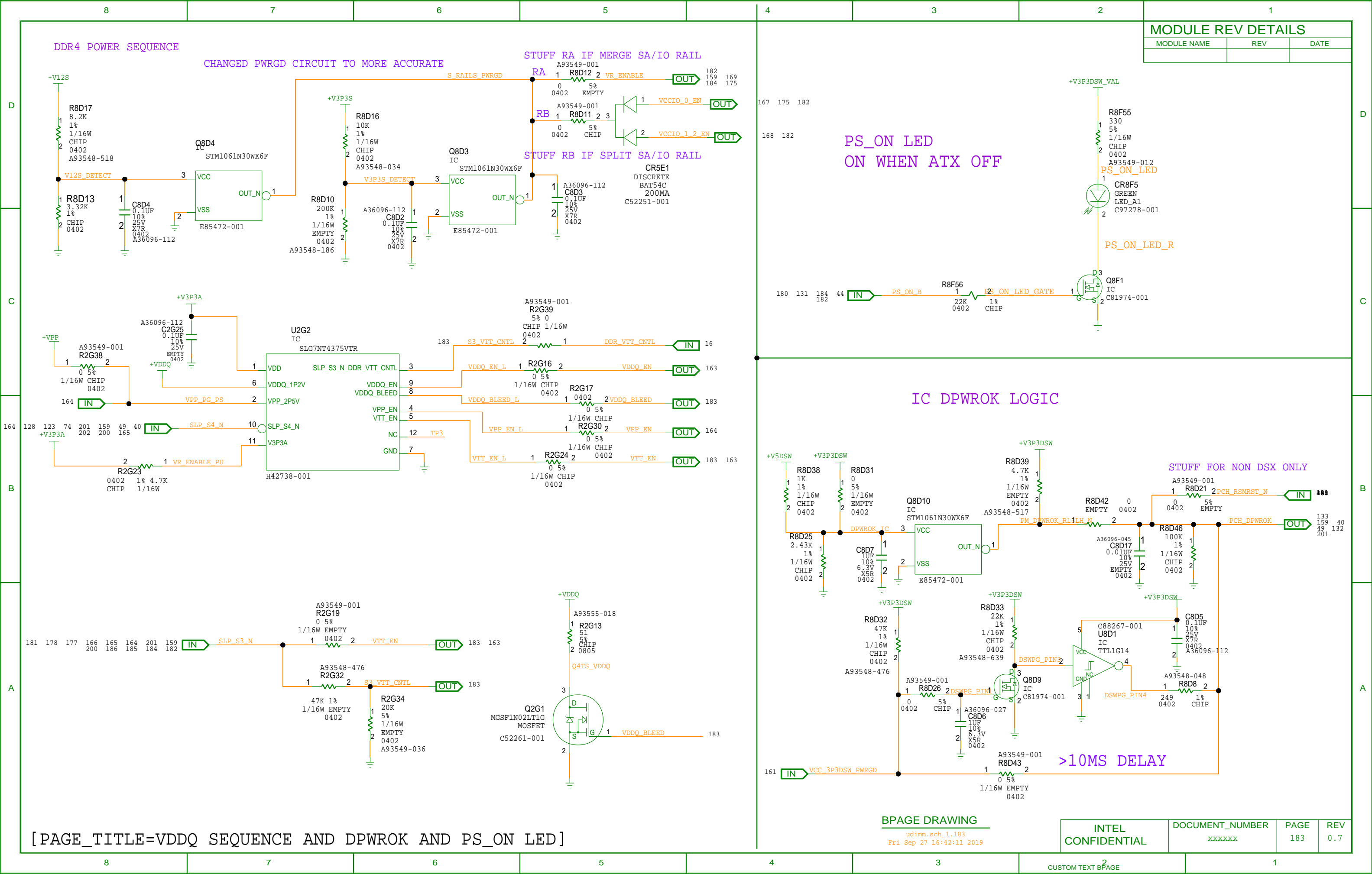
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Fri Sep 27 16:42:10 2019

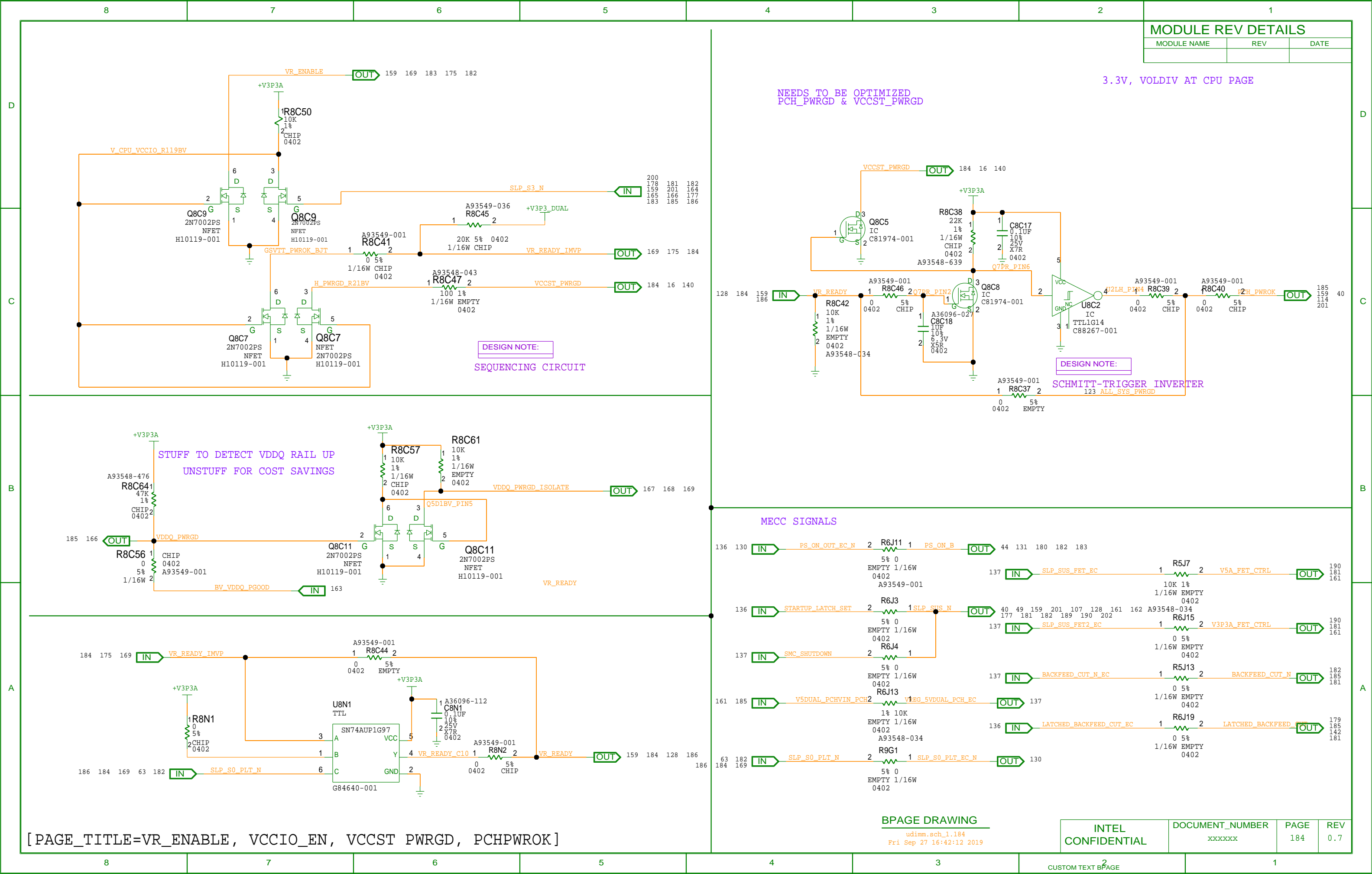
## MODULE REV DETAILS

MODULE NAME	REV	DATE

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MODULE NAME	REV	DATE

## LATCHED\_BACKFEED CUT LOGIC



	BFC	LBFC	BFC_DSW
S0	0	0	0
S3	1	1	1
S4/S5	1	0	1
DS4/DS5	0	0	1



## B



8	7	6	5	4	3	2 CUSTOM TEXT B PAGE	1
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udimm.sch_1.185
Fri Sep 27 16:42:13 2019
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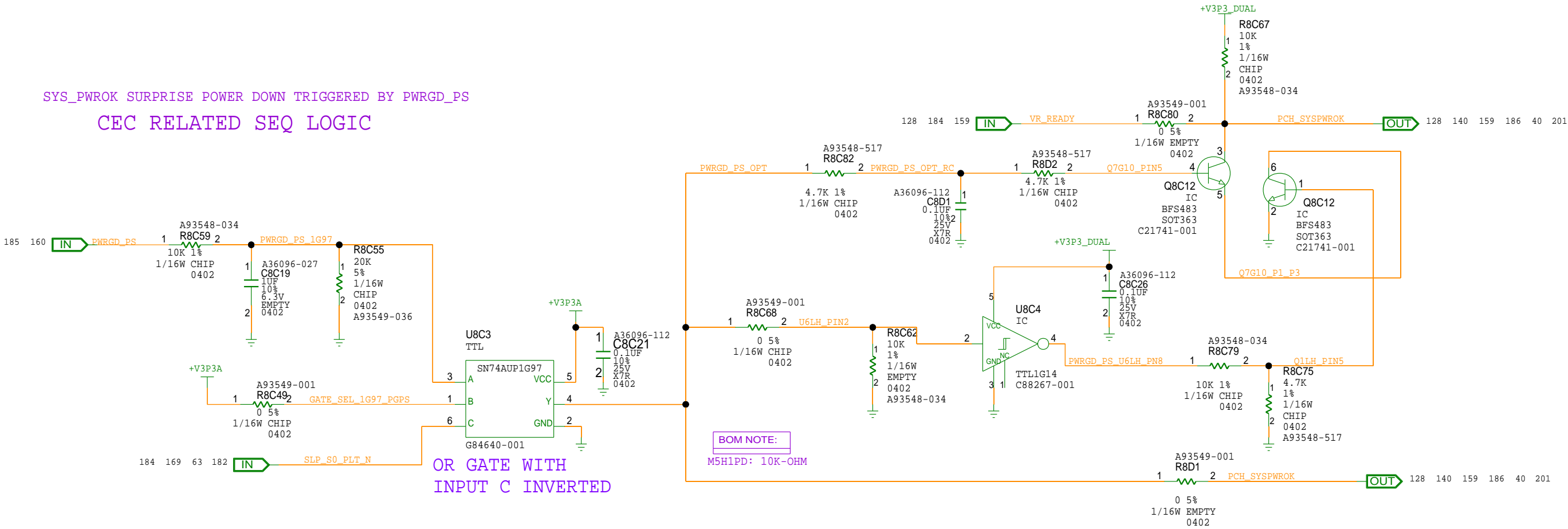
PAGE	REV
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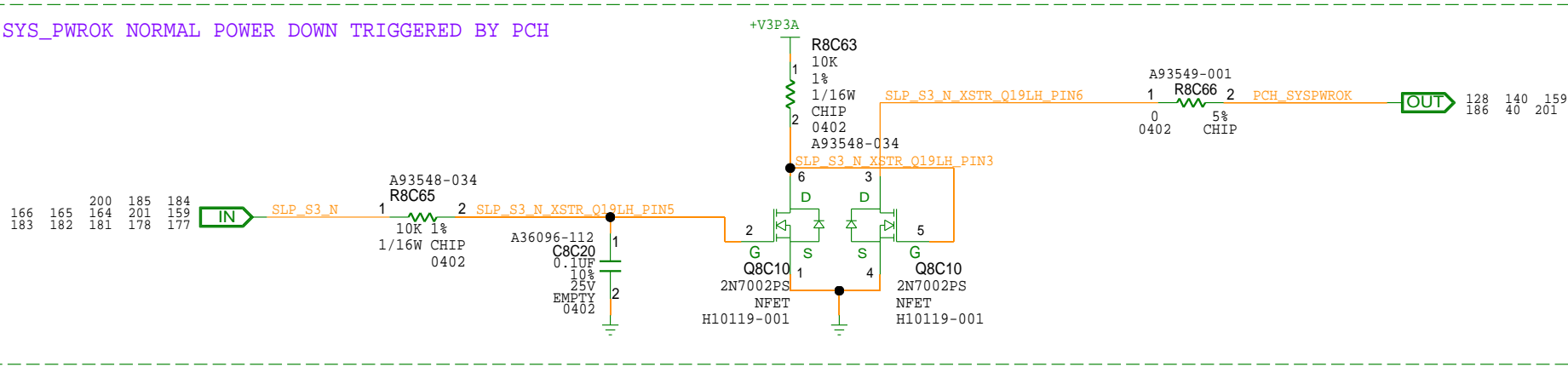
MODULE REV DETAILS

MODULE NAME	REV	DATE

SYS\_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD\_PS  
CEC RELATED SEQ LOGIC



SYS\_PWROK NORMAL POWER DOWN TRIGGERED BY PCH



BPAGE DRAWING

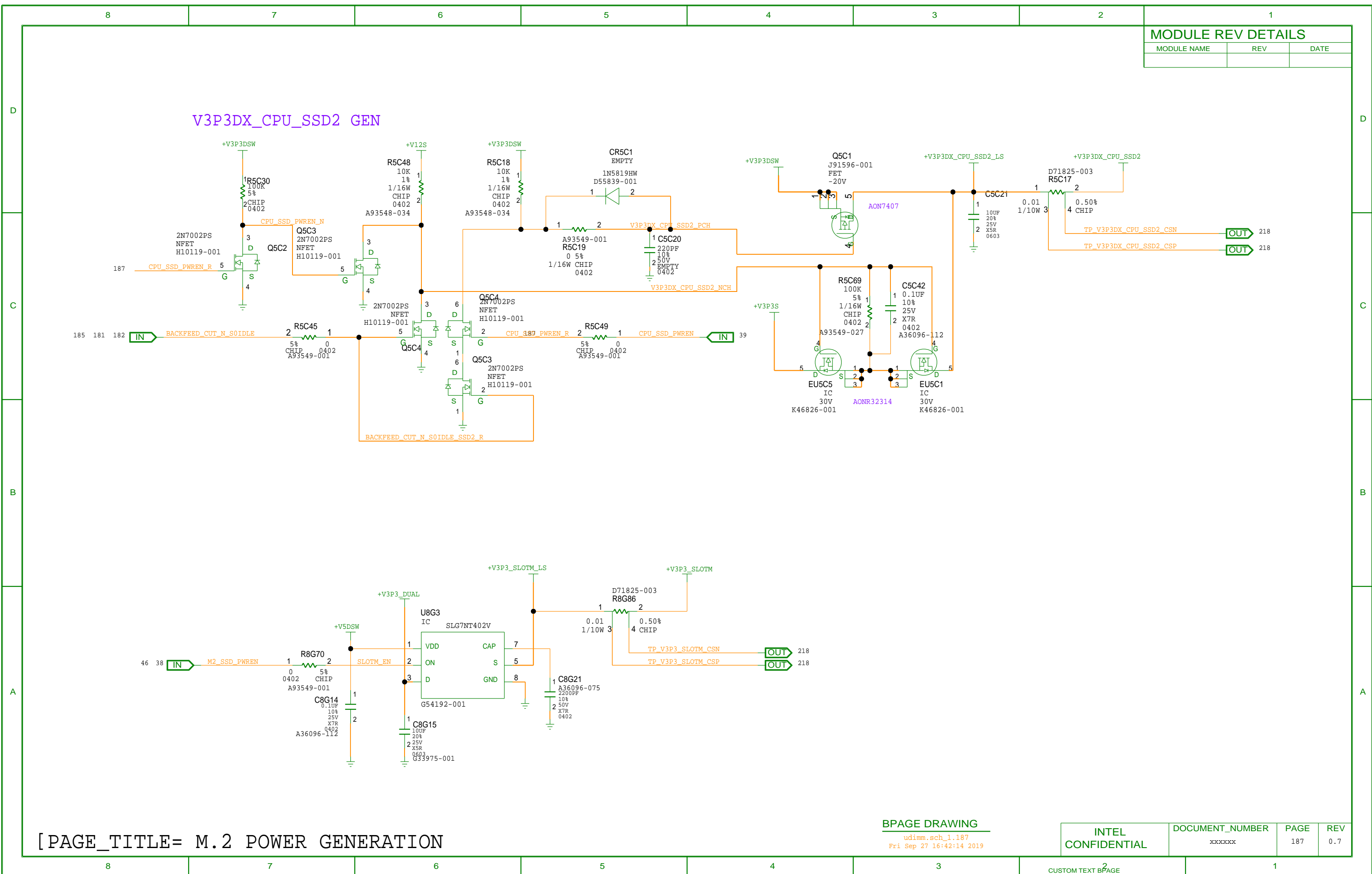
udimm.sch\_1.186  
Fri Sep 27 16:42:13 2019

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CONFIDENTIAL

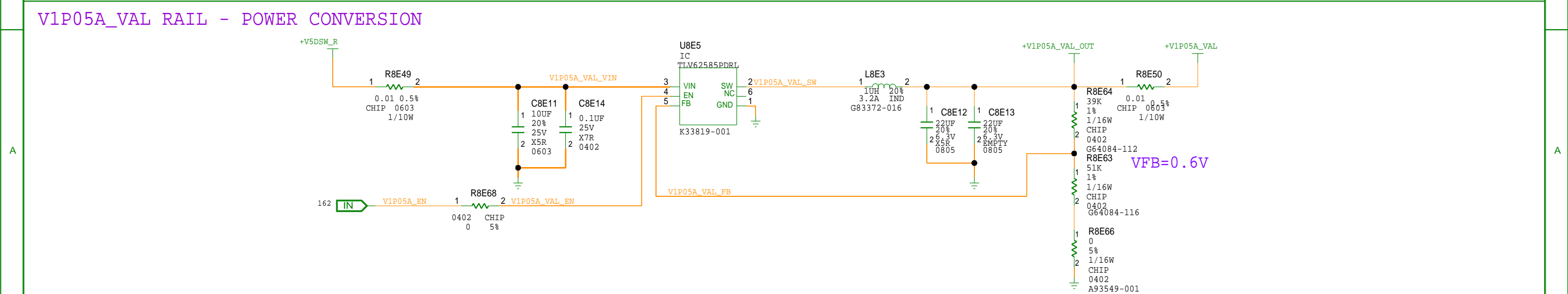
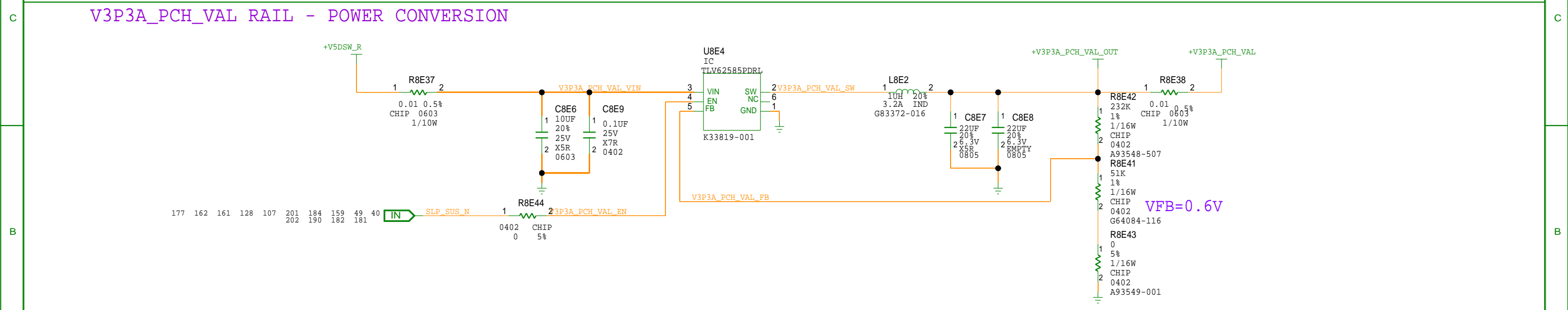
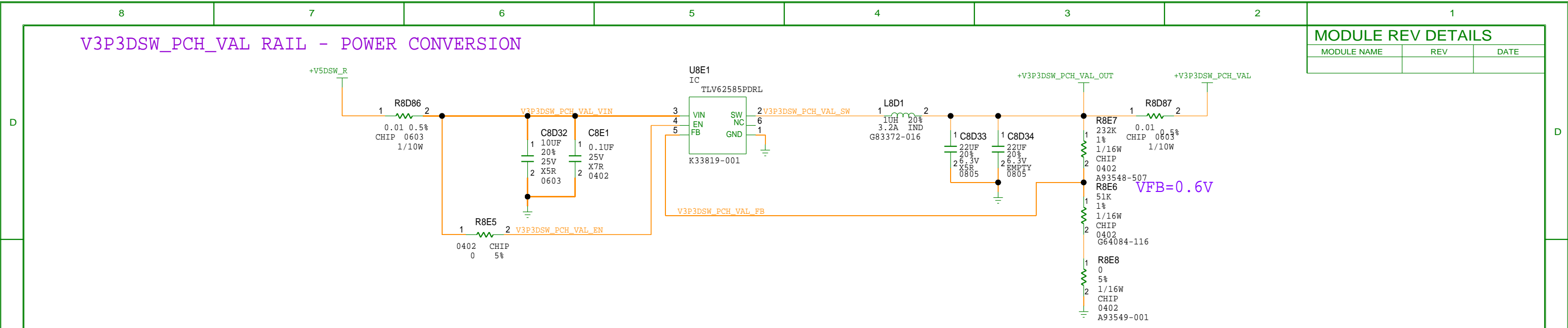
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REV  
0.7







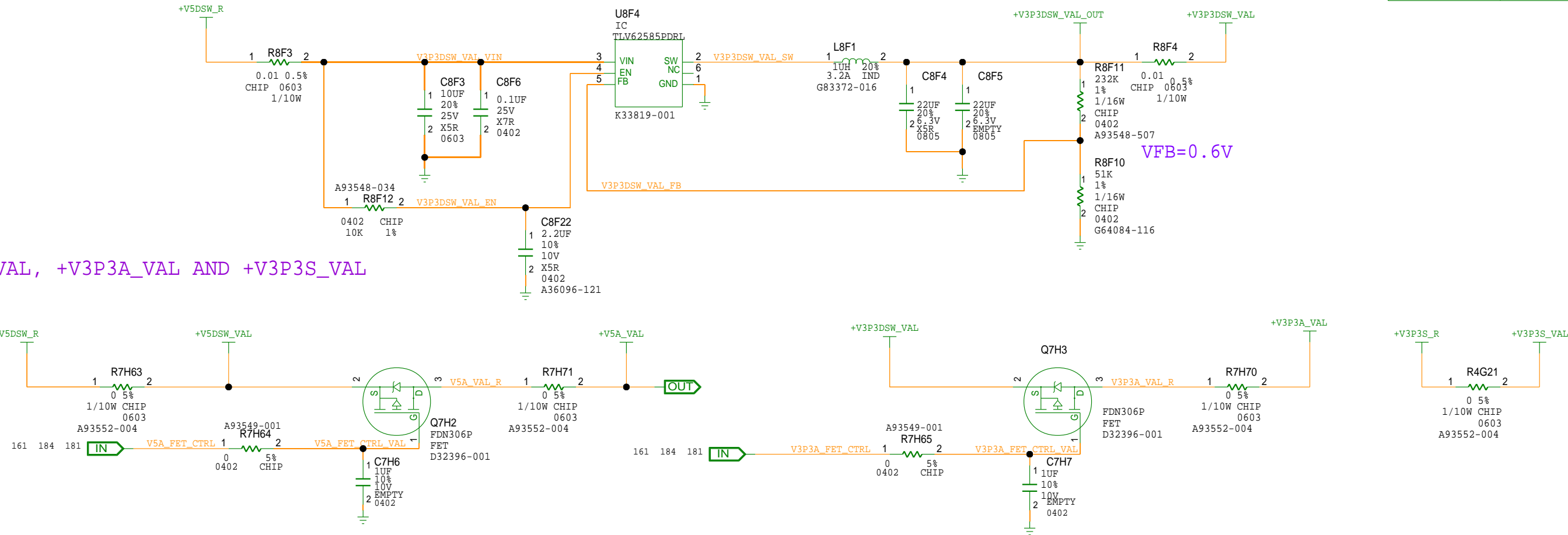


V3P3DSW VAL RAIL - POWER CONVERSION

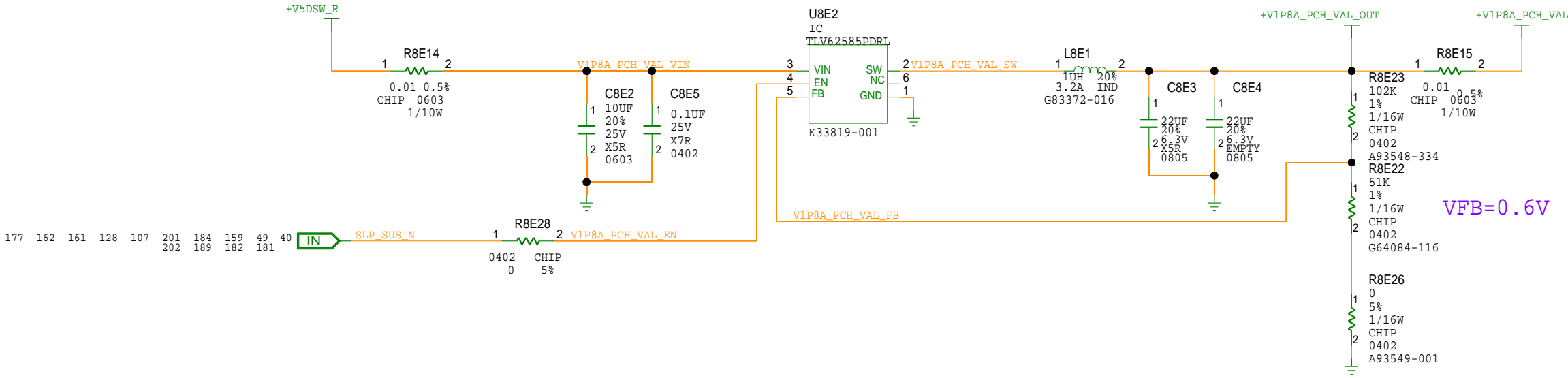
MODULE REV DETAILS

MODULE NAME	REV	DATE

+V5A\_VAL, +V3P3A\_VAL AND +V3P3S\_VAL



V1P8A\_PCH\_VAL RAIL - POWER CONVERSION

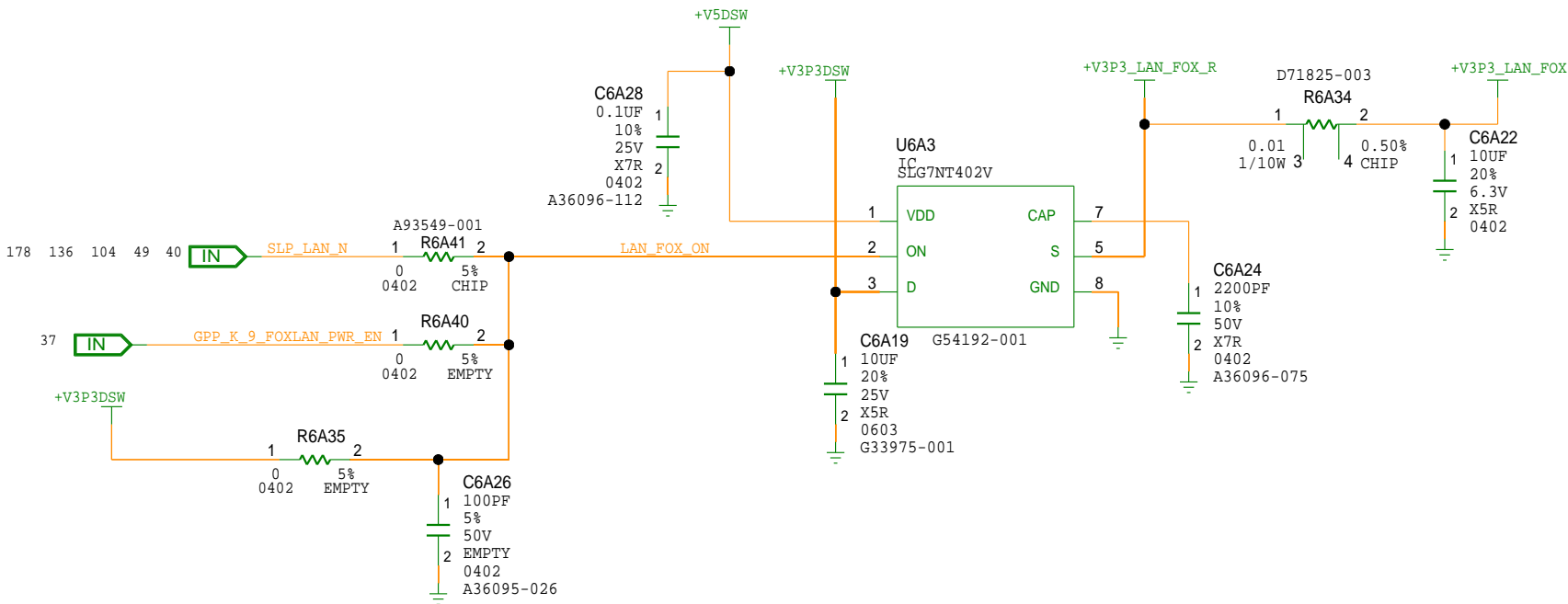




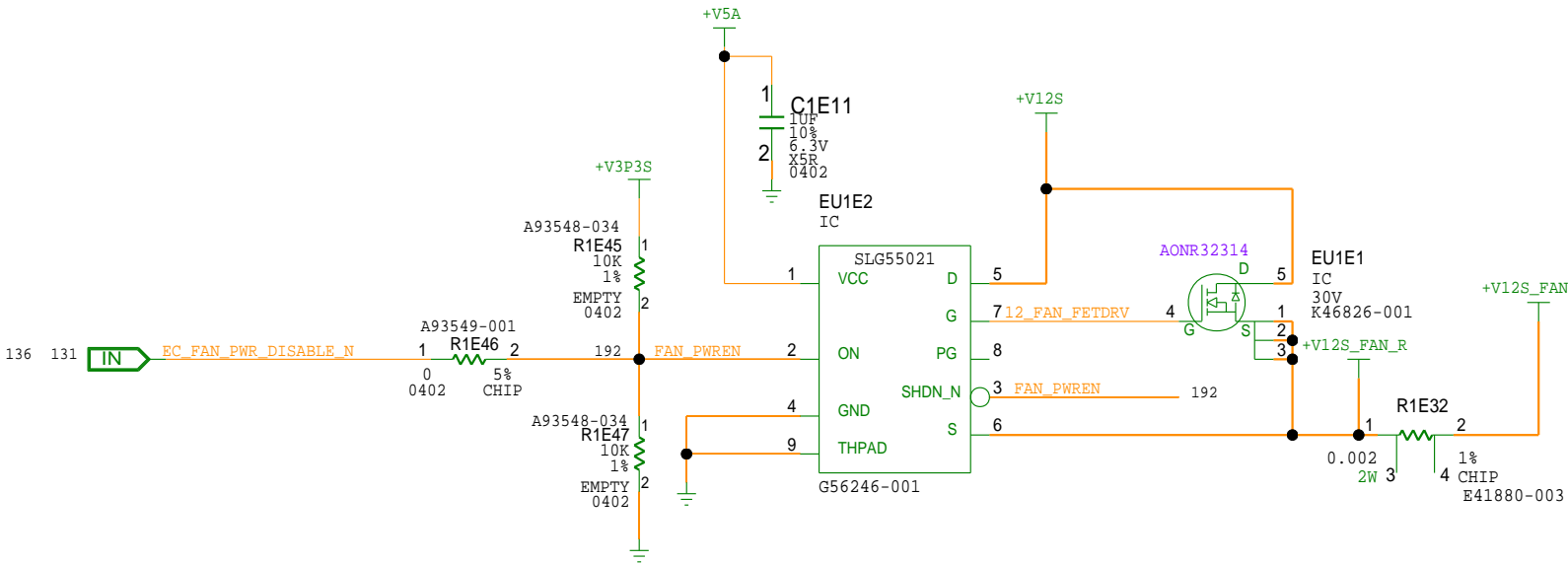
MODULE REV DETAILS

MODULE NAME	REV	DATE

FOXVILLE LAN POWER



12V FAN POWER

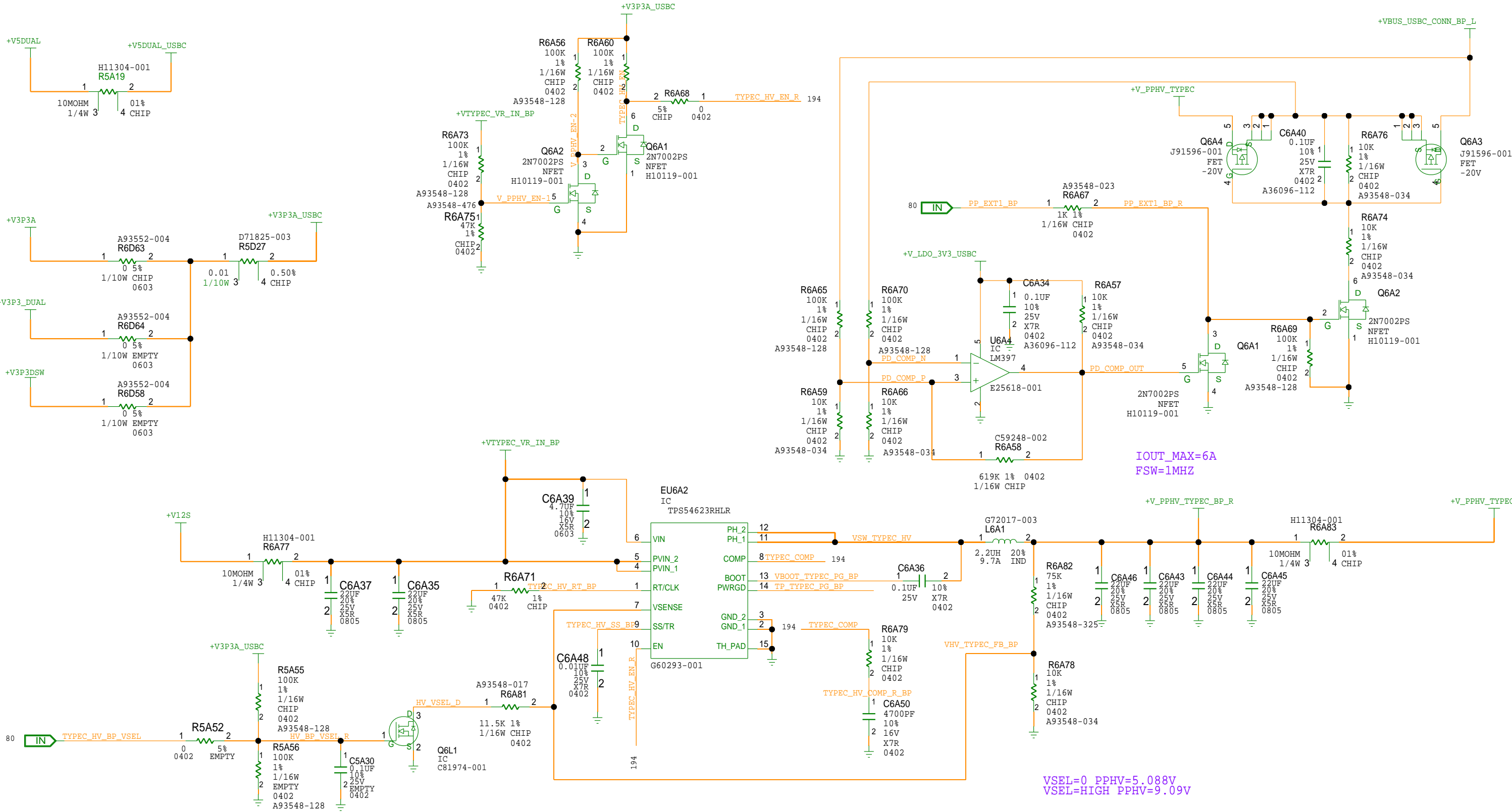




TYPE-C POWER

MODULE REV DETAILS

MODULE NAME	REV	DATE

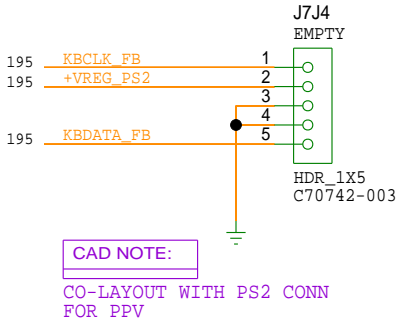
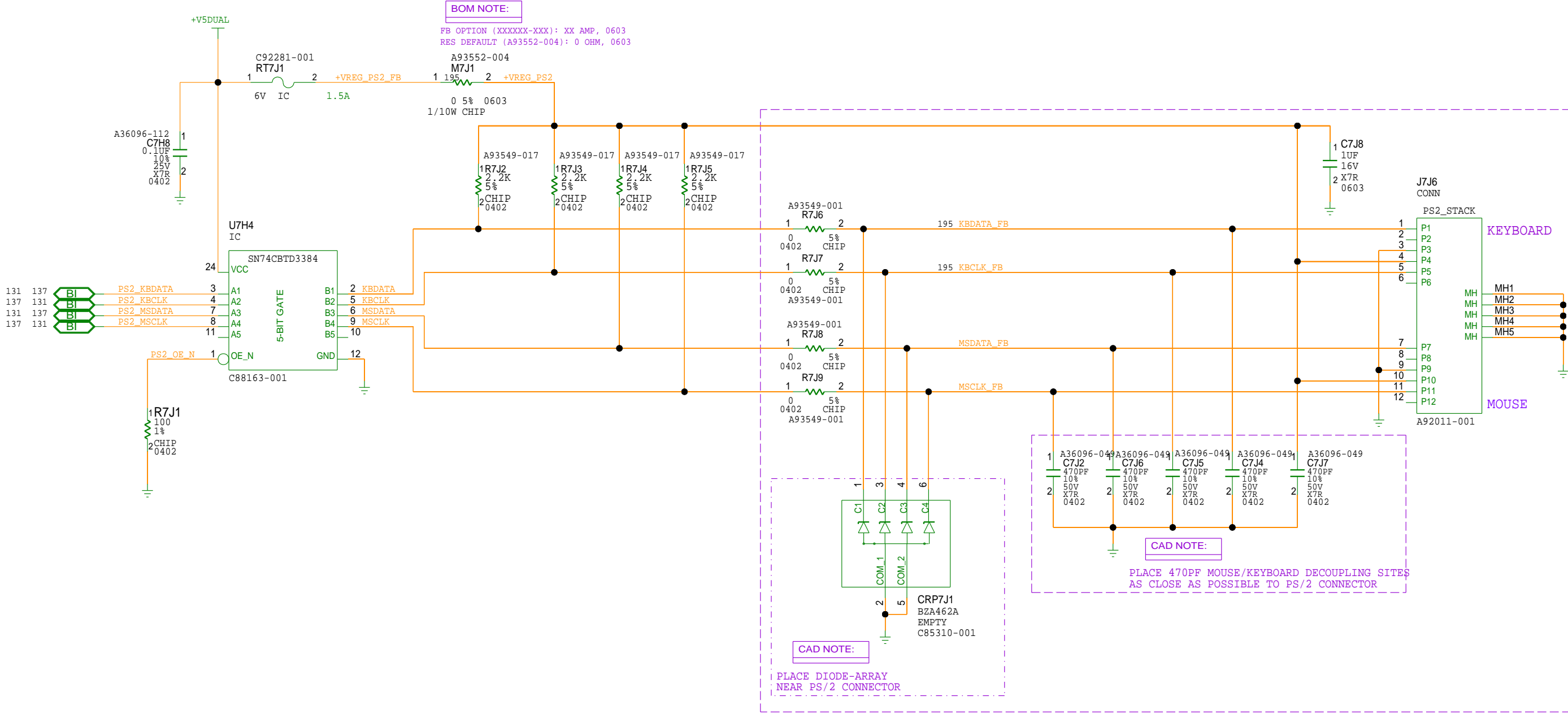


IOUT\_MAX=6A  
FSW=1MHZ

VSEL=0 PPHV=5.088V  
VSEL=HIGH PPHV=9.09V

MODULE REV DETAILS

MODULE NAME	REV	DATE









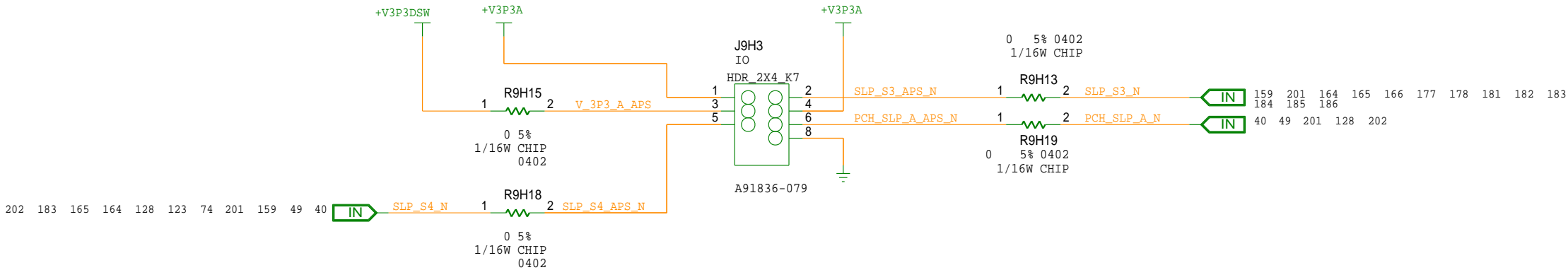
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														MODULE REV DETAILS			
														MODULE NAME		REV	DATE



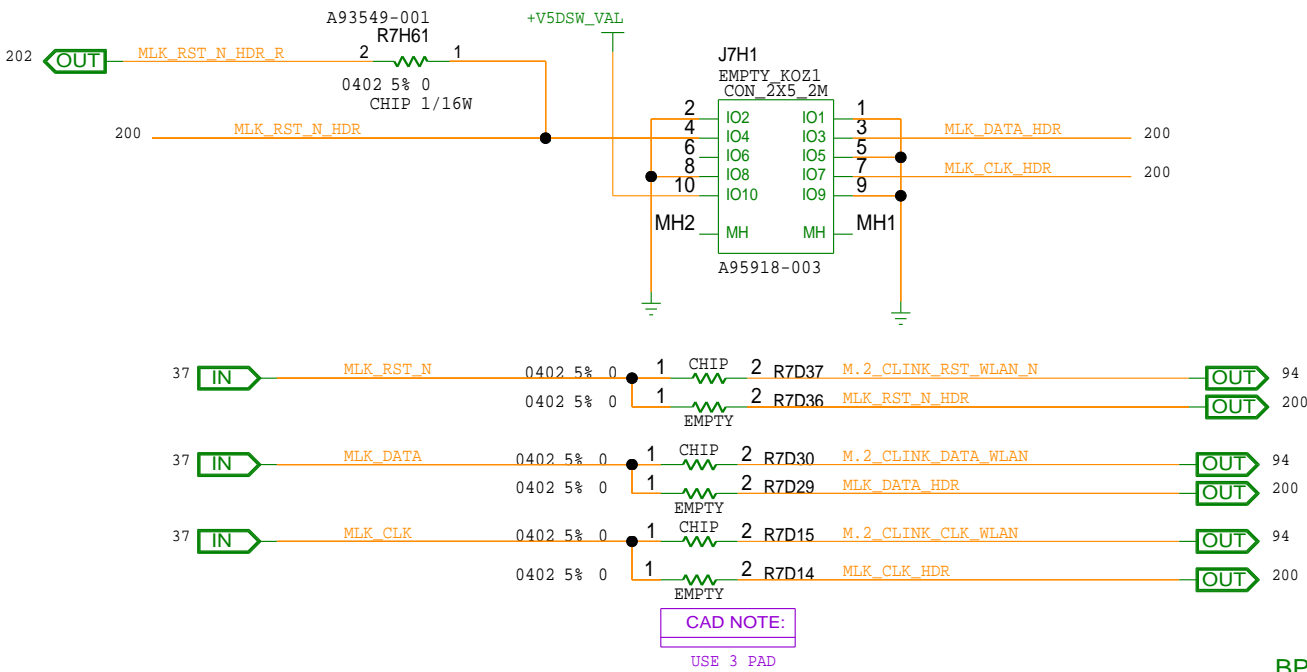
MODULE REV DETAILS

MODULE NAME	REV	DATE

APS HEADER



MLINK HEADER



CAD NOTE:  
USE 3 PAD

[PAGE\_TITLE=EV - DEBUG HEADERS]

BPAGE DRAWING

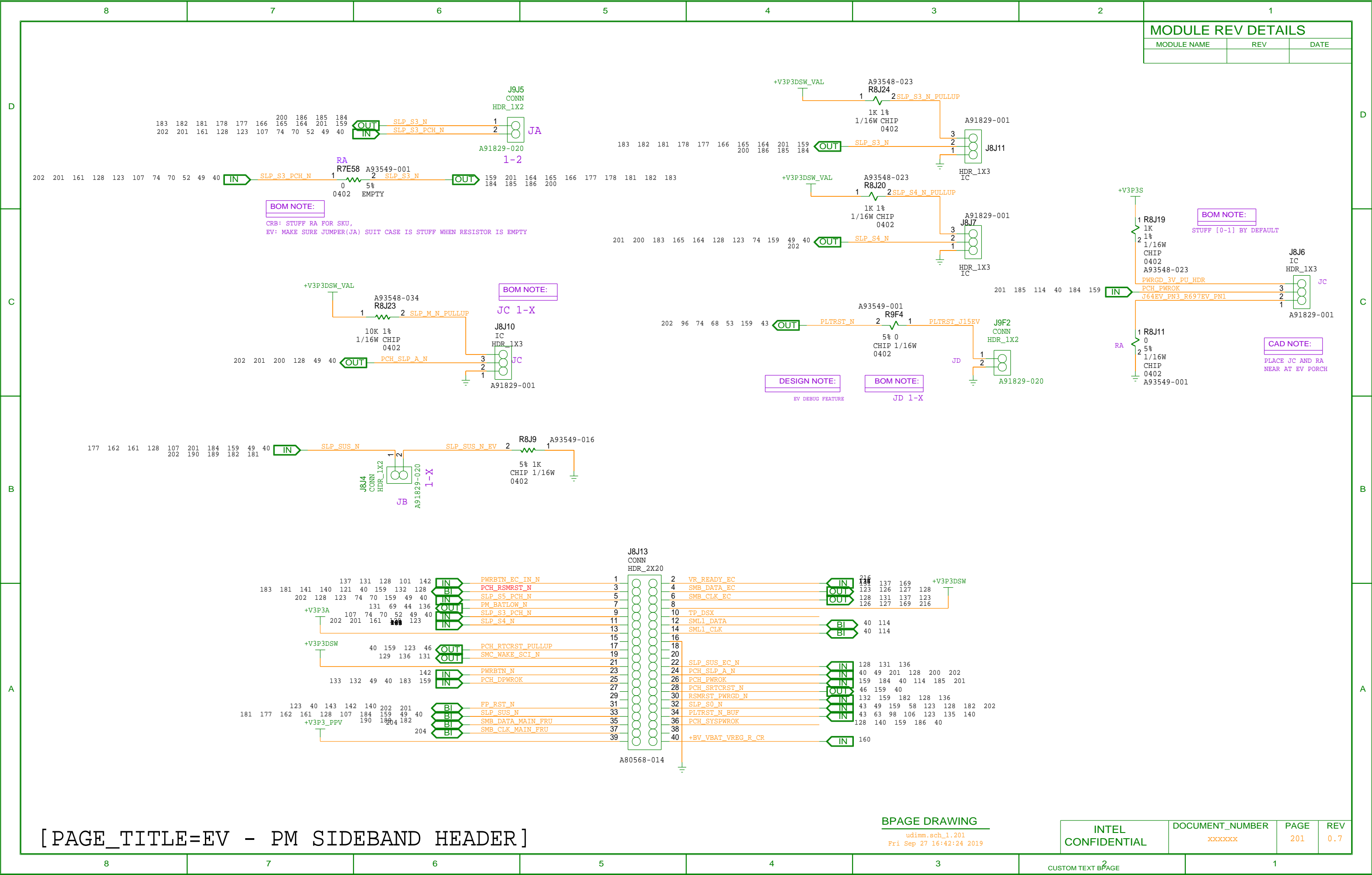
udimm.sch\_1.200  
Fri Sep 27 16:42:23 2019

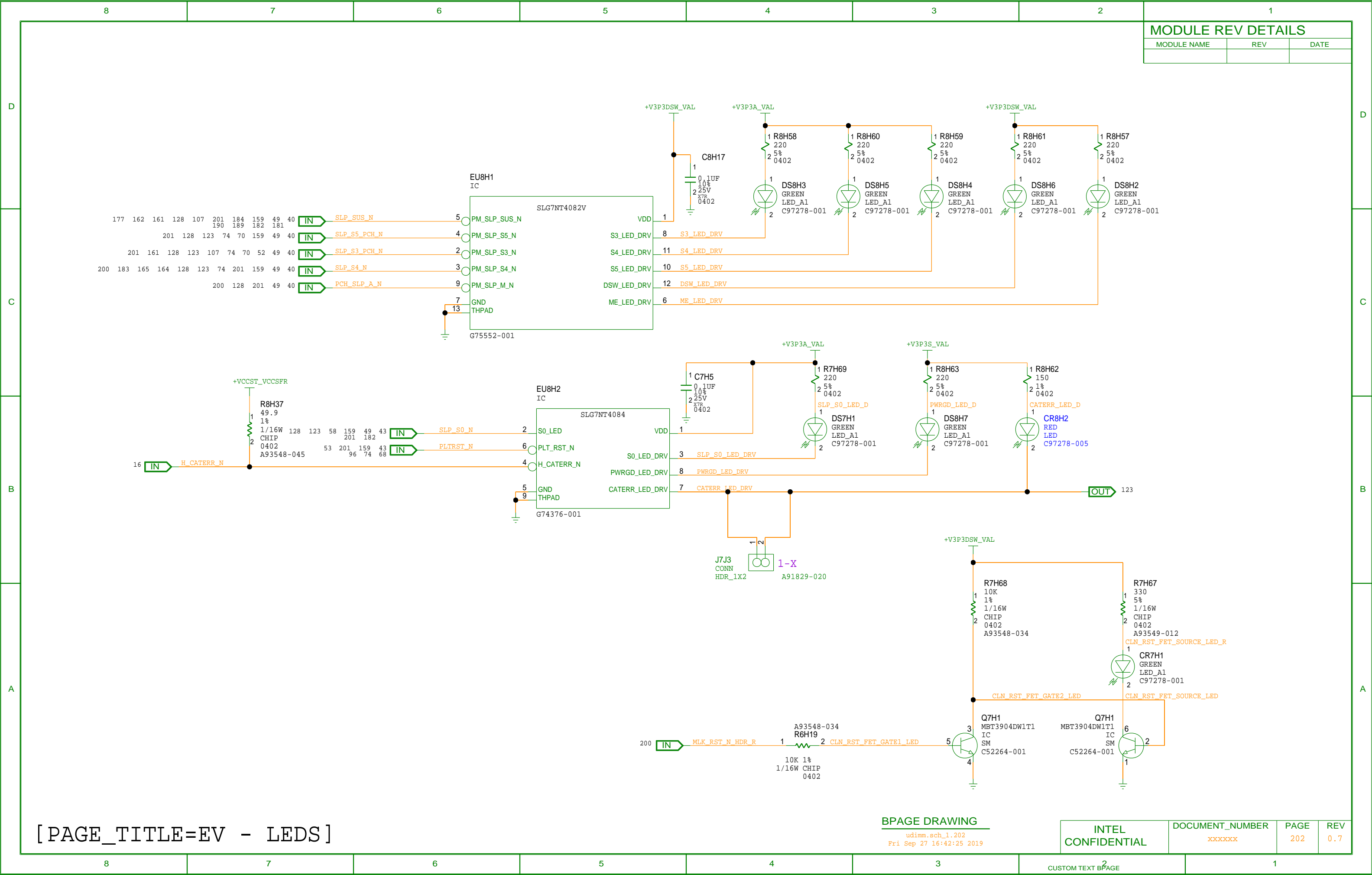
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CONFIDENTIAL

DOCUMENT\_NUMBER  
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PAGE  
200

REV  
0.7



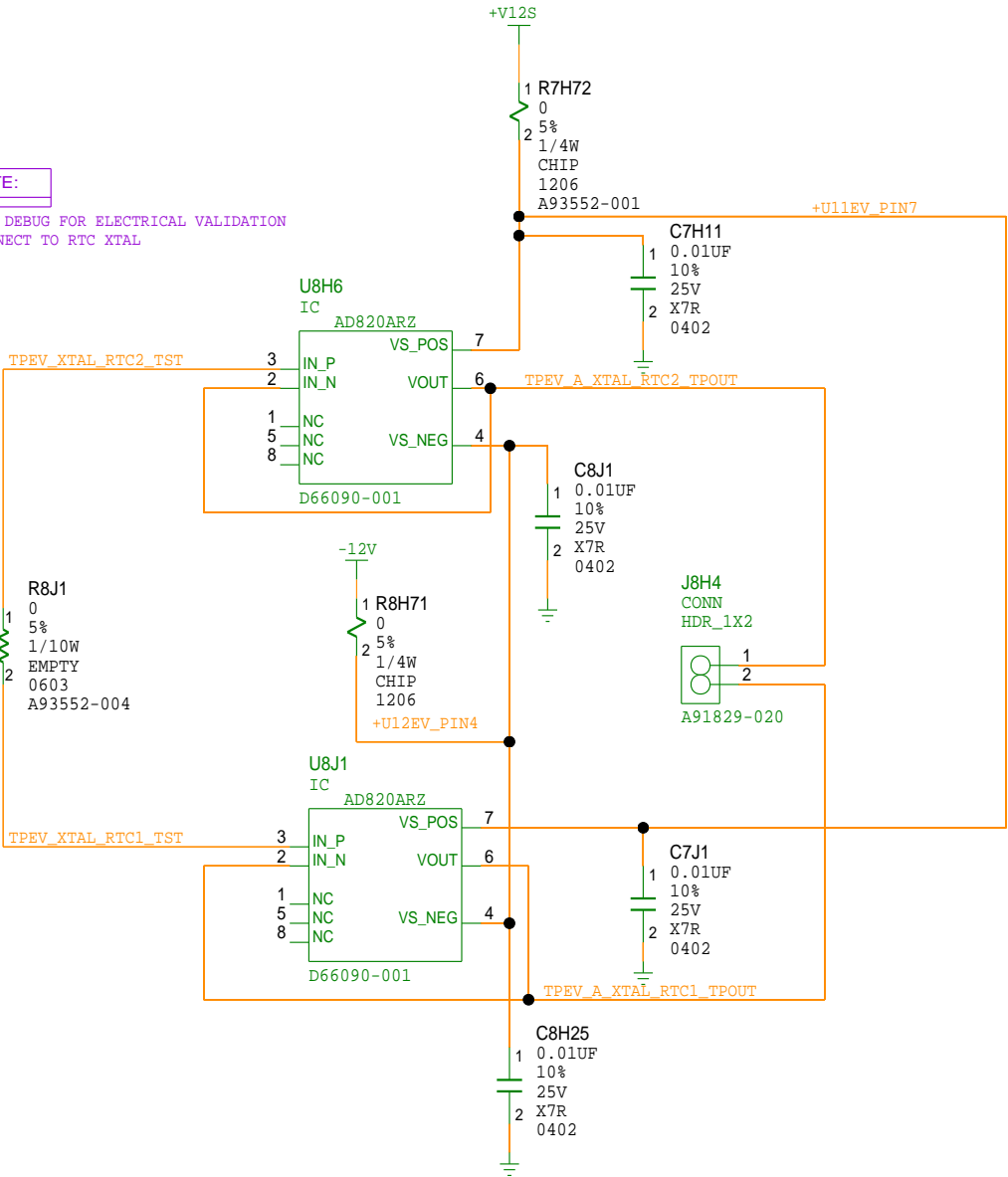


MODULE REV DETAILS

MODULE NAME	REV	DATE

DESIGN NOTE:  
RTC CHECKING AND DEBUG FOR ELECTRICAL VALIDATION  
BLUE-WIRE TO CONNECT TO RTC XTAL

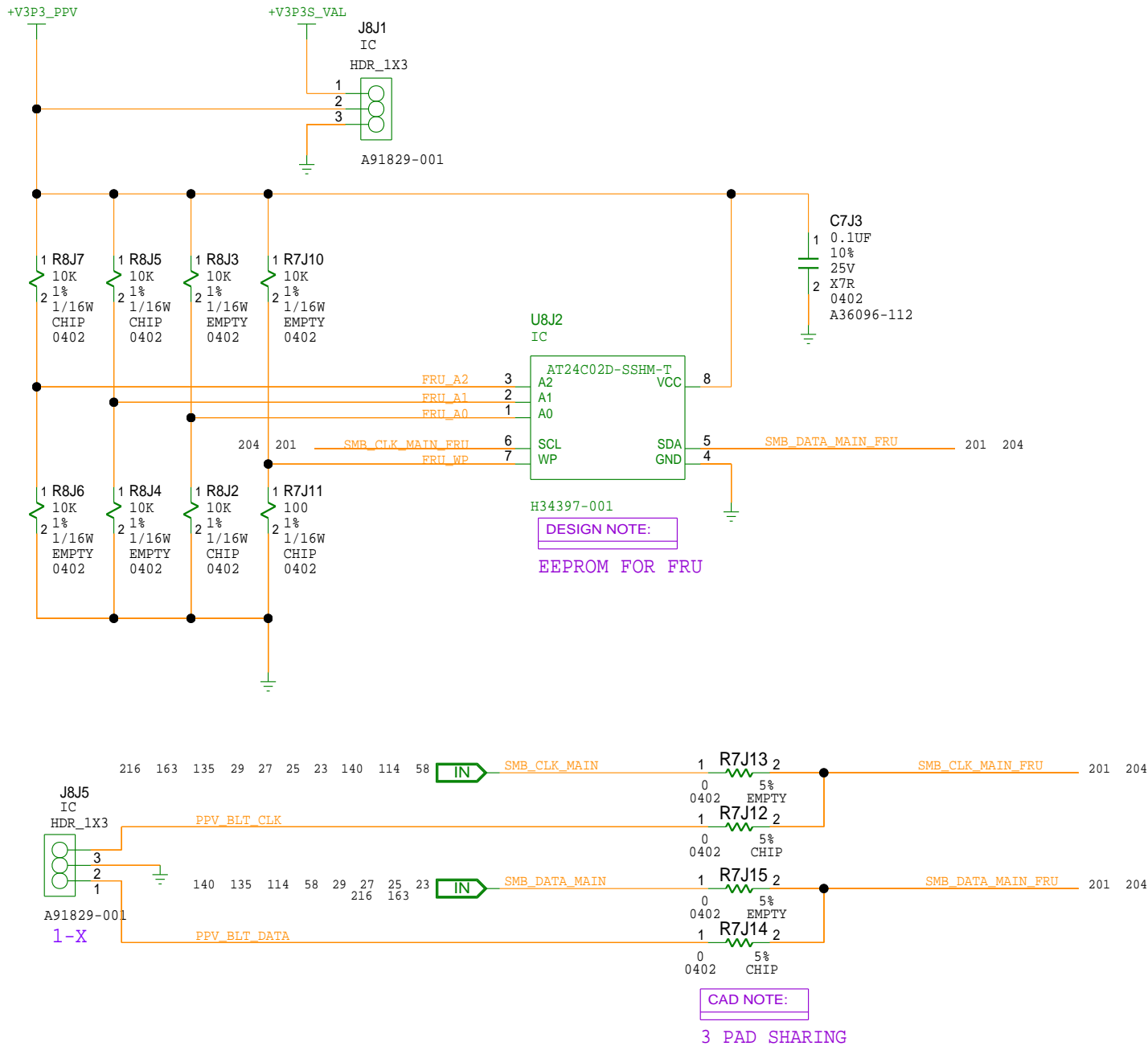
DESIGN NOTE:  
R4J5EV IS PAD FOR BLUE WIRE





MODULE REV DETAILS

MODULE NAME	REV	DATE





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														MODULE REV DETAILS						
														MODULE NAME	REV	DATE				
D															D					
C															C					
B															B					
A															A					
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8		7		6		5		4		3		2		1						
												CUSTOM TEXT BPAGE								













8		7		6		5		4		3		2		1						
														MODULE REV DETAILS						
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D															D					
C															C					
B															B					
A															A					
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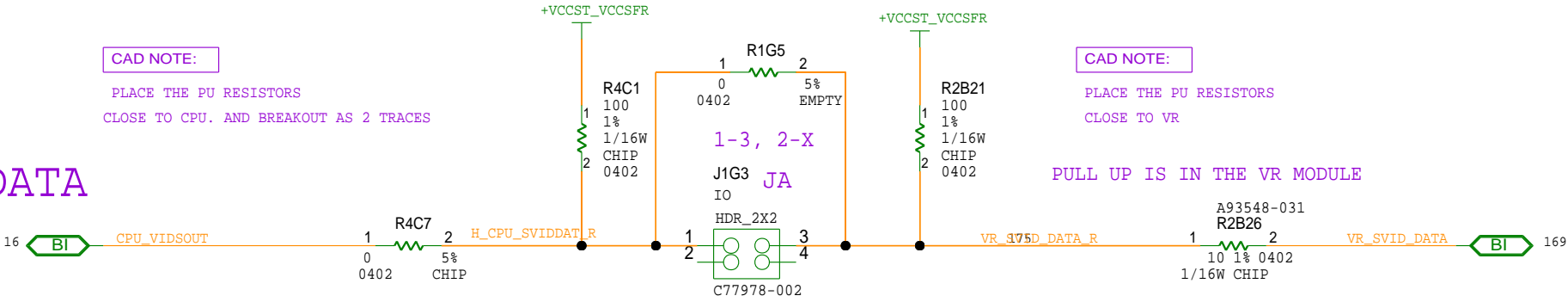


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CUSTOM TEXT B														2		PAGE		1	
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udimm.sch_1.214 Fri Sep 20 11:44:35 2019																			
B PAGE DRAWING																			

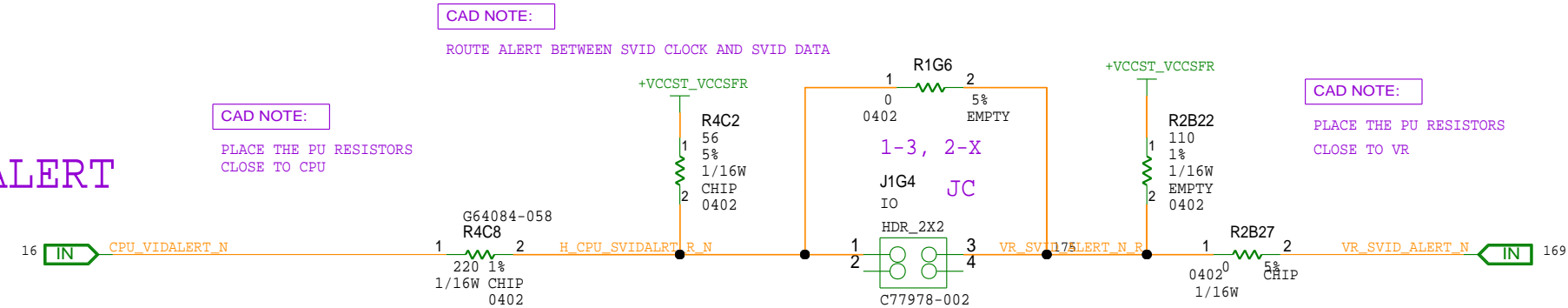
MODULE REV DETAILS

MODULE NAME	REV	DATE

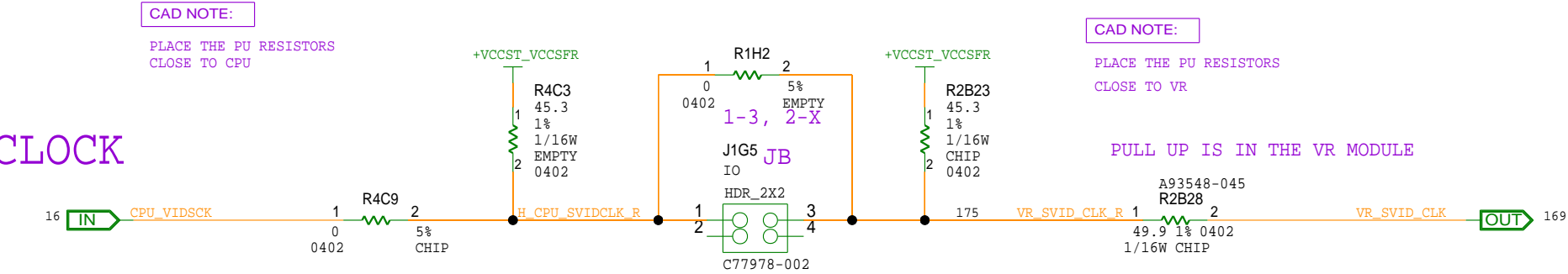
SVID DATA



SVID ALERT



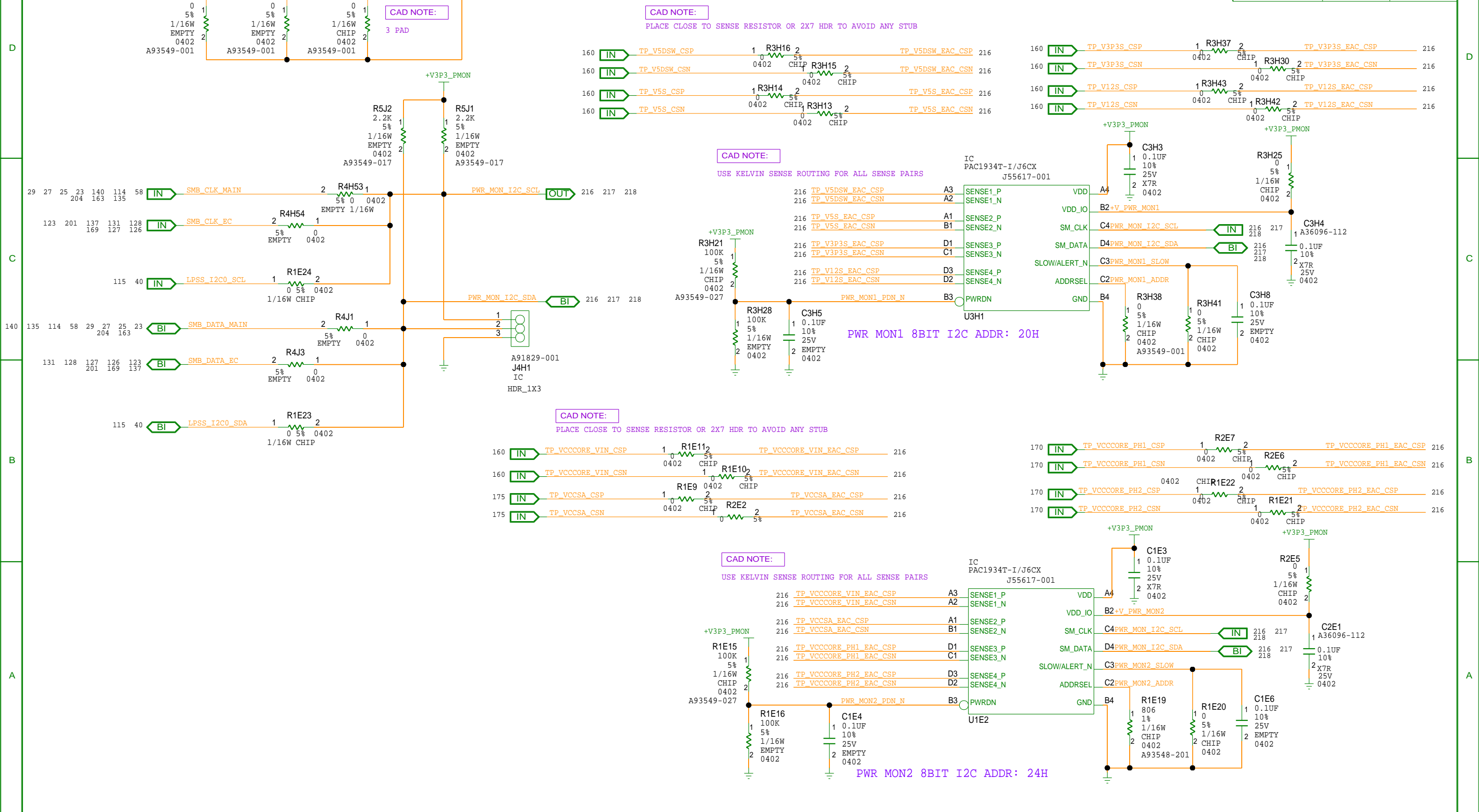
SVID CLOCK

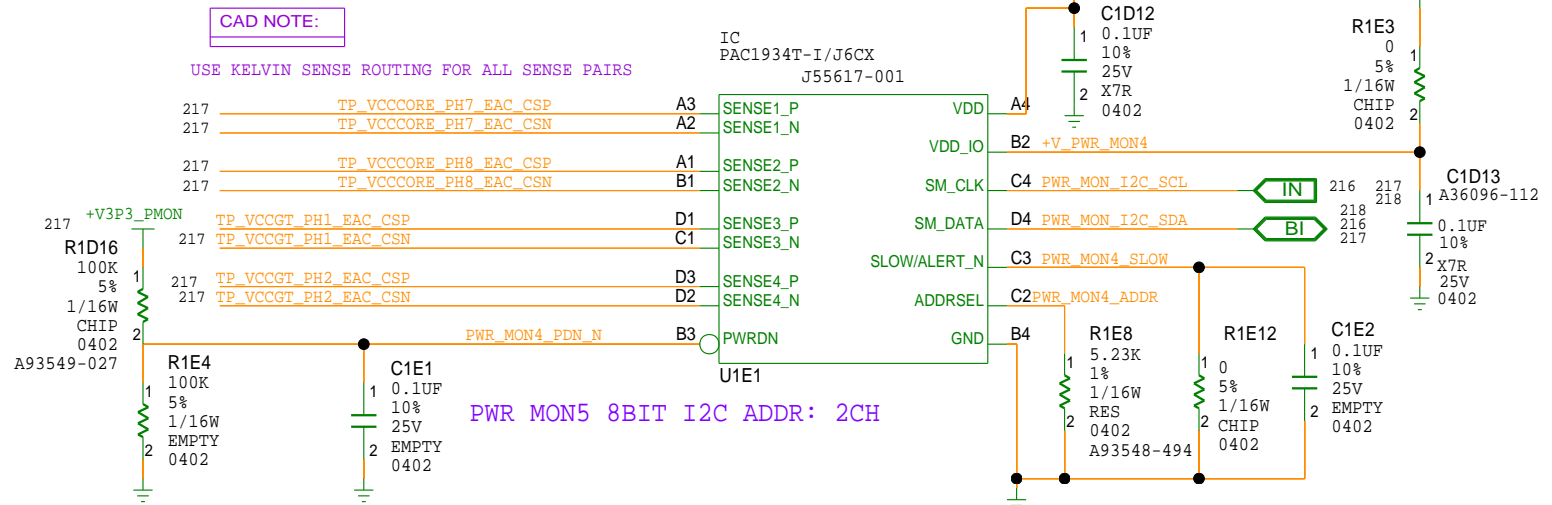


DESIGN NOTE:

STUFFING DETAILS ON THE BOARD

	JA	JB	JC
DEFAULT	1-3, 2-X	1-3, 2-X	1-3, 2-X

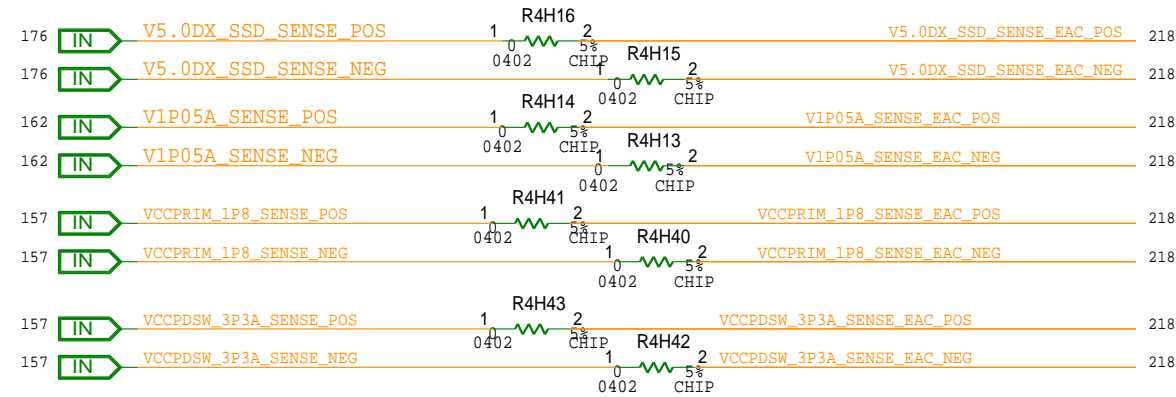




MODULE NAME	REV	DATE

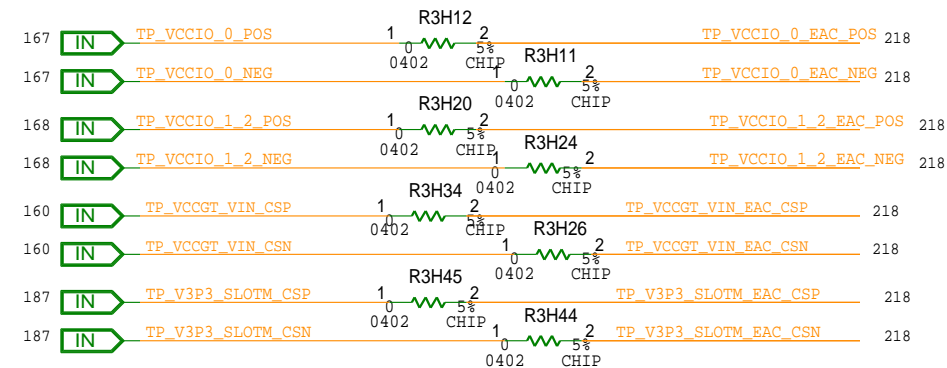
**CAD NOTE:**

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



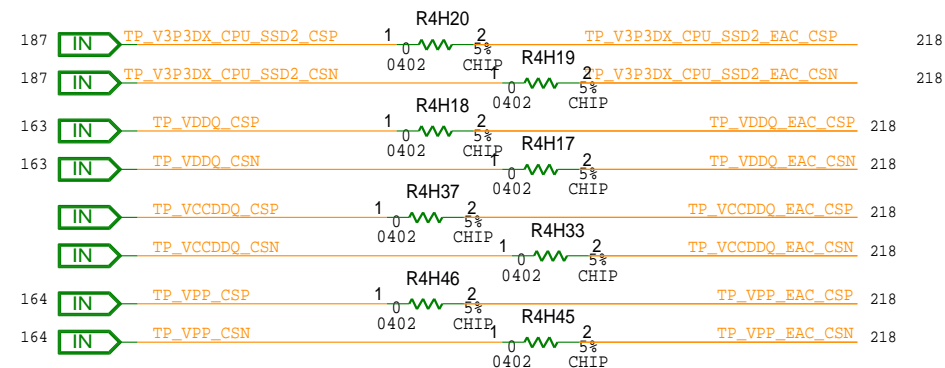
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



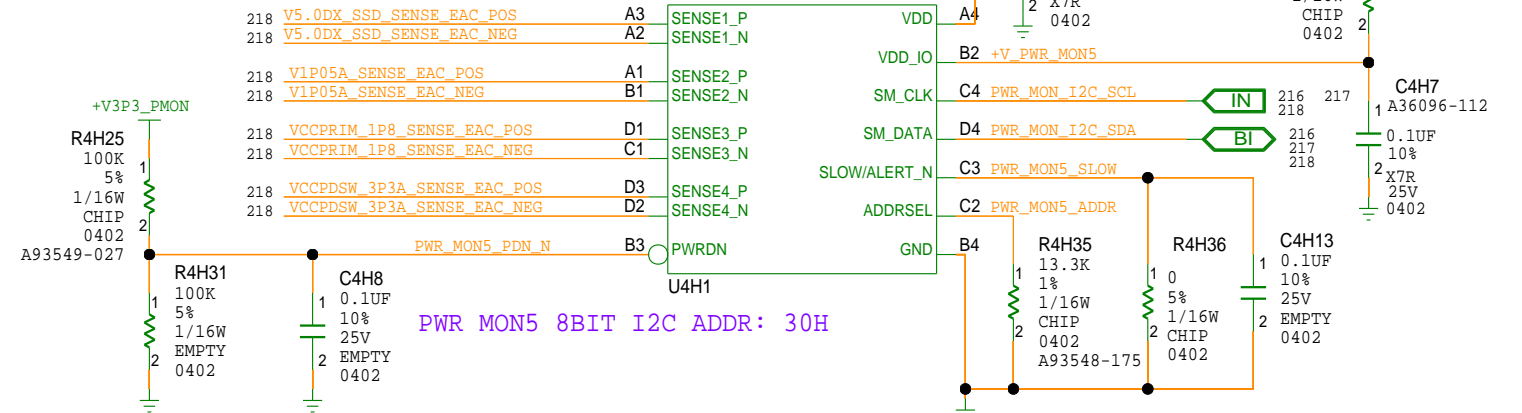
CAD NOTE:

PLACE CLOSE TO SENSE RESISTOR OR 2X7 HDR TO AVOID ANY STUB



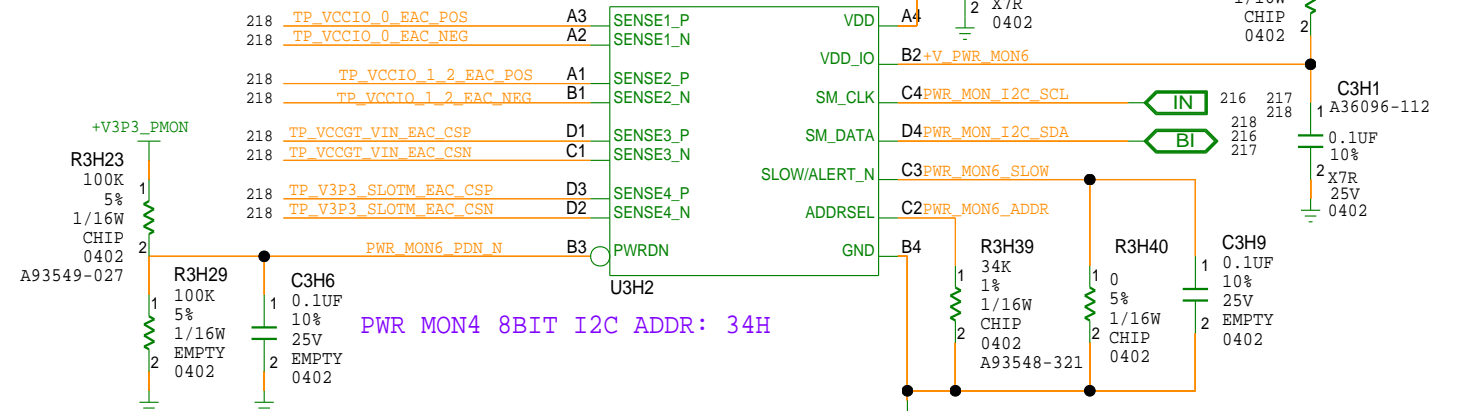
CAD NOTE:

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



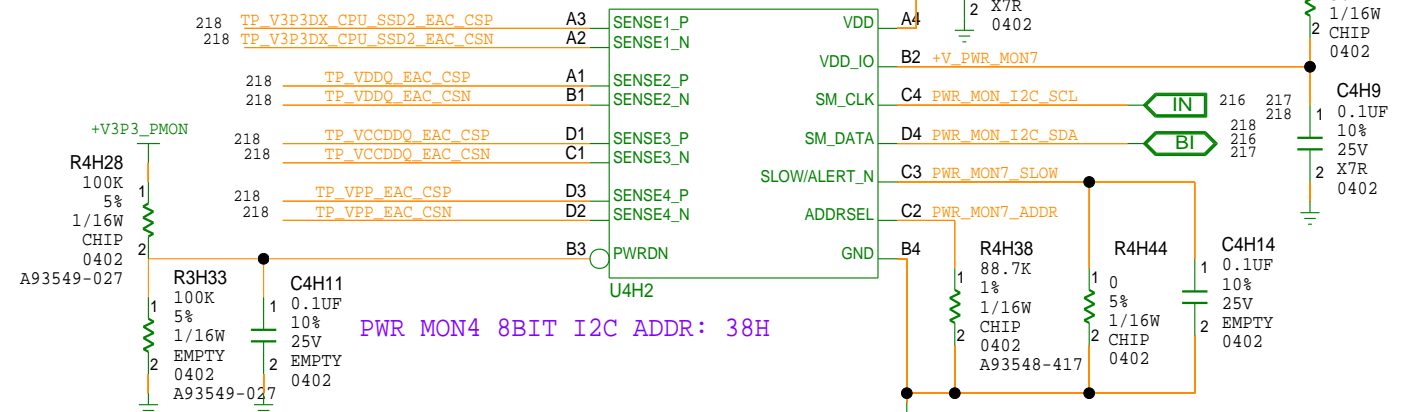
CAD NOTE:

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



**CAD NOTE:**

USE KELVIN SENSE ROUTING FOR ALL SENSE PAIRS



BPAGE DRAWING

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Fri Sep 27 16:42:36 2019



